

Ultra-Low Power Serial Persistent SRAM Memory

(AS1001101, AS1004101, AS1008101, AS1016101, AS3001101, AS3004101, AS3008101, AS3016101)

Features

- Interface
 - Serial Peripheral Interface SPI (1-1-1)
- Technology
 - 40nm pMTJ STT-MRAM
 - Virtually unlimited Endurance and Data Retention (see Endurance and Data Retention on page 25)
- Density
 - 1Mb, 4Mb, 8Mb, 16Mb
- Operating Voltage Range
 - V_{CC}: 1.71V – 2.00V
 - V_{CC}: 2.70V – 3.60V
- Operating Temperature Range
 - Industrial: -40°C to 85°C
 - Industrial Plus: -40°C to 105°C
- RoHS Compliant
- Packages
 - 8-pad WSON (5.0mm x 6.0mm)
 - 8-pin SOIC (5.2mm x 5.2mm)
- Data Protection
 - Hardware Based
 - Write Protect Pin (WP#)
 - Software Based
 - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect[2:0])
- Identification
 - 64-bit Unique ID
 - 64-bit User Programmable Serial Number
- Augmented Storage Array
 - 256-byte User Programmable and Lockable
- Supports HOLD# Functionality - Pause

Performance

Device Operation	Typical Values	Units
Frequency of Operation	10.0 (maximum)	MHz
Standby Current	2.2 (typical)	μA
Active Read Current @1.8V 10MHz	2.0 (typical)	mA
Active Write Current @1.8V 10MHz	10.0 (typical)	mA

Table of Contents

Features	1
Performance	1
Table of Contents	2
General Description	4
Ordering Options	5
Valid Combinations — Standard	5
Signal Description and Assignment	11
Package Options	12
8-Pad WSON (Top View)	12
8-Pin SOIC (Top View)	12
Package Drawings	13
8-Pad WSON	13
8-Pin SOIC	14
Architecture	15
Device Initialization	16
Memory Map	18
Augmented Storage Array Map	18
Register Map	19
Status Register / Device Protection Register (Read/Write)	19
Status register is a legacy SPI register and contains options for enabling/disabling data protection.....	19
Device Identification Register (Read Only)	21
Serial Number Register (Read/Write)	21
Unique Identification Register (Read Only)	21
Instruction Set	22
Instruction Description and Structures	23
Electrical Specifications	25
CS# Operation & Timing	29
Command, Address and Data Input Operation & Timing	30
Data Output Operation & Timing	31

WP# Operation & Timing	32
HOLD# Operation & Timing	33
Thermal Resistance	34
Product Use Limitations	35
Limited Warranty	35
Revision History	36

General Description

ASxxxx101 is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in density ranging from 1Mbit to 16Mbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile.

Figure 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually infinite endurance and data retention, and, scalable non-volatile memory technology.

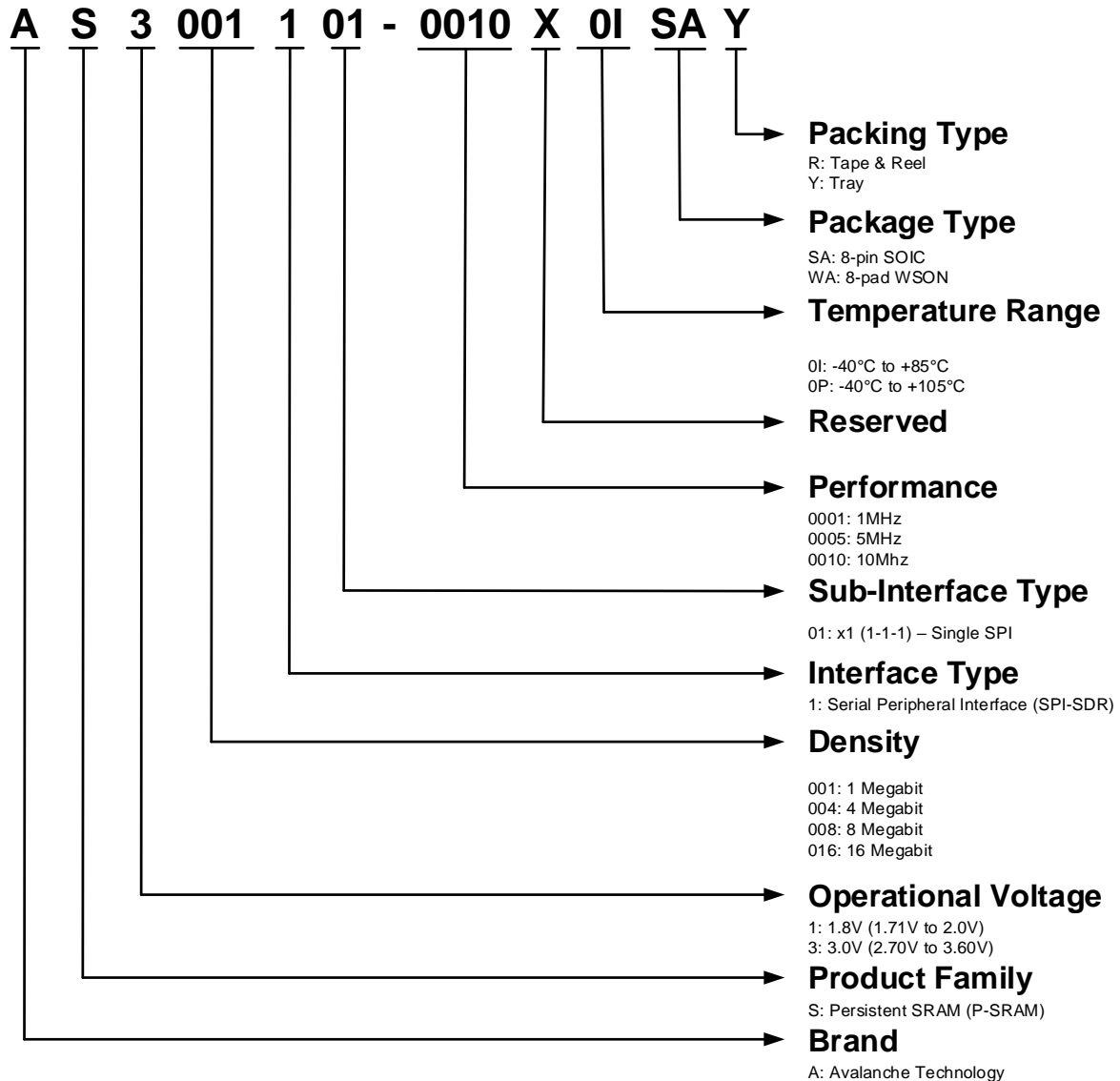
ASxxxx101 has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (Low to High) or falling (High to Low) edge of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

ASxxxx101 is available in small footprint 8-pad WSON and 8-pin SOIC packages. These packages are compatible with similar low-power volatile and non-volatile products.

ASxxxx101 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1: Valid Combinations List

Valid Combinations – 1MHz				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
AS1001101-0001X	0I, 0P	SA, WA	R, Y	AS1001101-0001X0ISAR
				AS1001101-0001X0ISAY
				AS1001101-0001X0PSAR
				AS1001101-0001X0PSAY
				AS1001101-0001X0IWAR
				AS1001101-0001X0IWAY
				AS1001101-0001X0PWAR
				AS1001101-0001X0PWAY
AS1004101-0001X	0I, 0P	SA, WA	R, Y	AS1004101-0001X0ISAR
				AS1004101-0001X0ISAY
				AS1004101-0001X0PSAR
				AS1004101-0001X0PSAY
				AS1004101-0001X0IWAR
				AS1004101-0001X0IWAY
				AS1004101-0001X0PWAR
				AS1004101-0001X0PWAY
AS1008101-0001X	0I, 0P	SA, WA	R, Y	AS1008101-0001X0ISAR
				AS1008101-0001X0ISAY
				AS1008101-0001X0PSAR
				AS1008101-0001X0PSAY
				AS1008101-0001X0IWAR
				AS1008101-0001X0IWAY
				AS1008101-0001X0PWAR
				AS1008101-0001X0PWAY
AS1016101-0001X	0I, 0P	SA, WA	R, Y	AS1016101-0001X0ISAR
				AS1016101-0001X0ISAY
				AS1016101-0001X0PSAR
				AS1016101-0001X0PSAY
				AS1016101-0001X0IWAR
				AS1016101-0001X0IWAY
				AS1016101-0001X0PWAR
				AS1016101-0001X0PWAY
AS3001101-0001X	0I, 0P	SA, WA	R, Y	AS3001101-0001X0ISAR
				AS3001101-0001X0ISAY
				AS3001101-0001X0PSAR
				AS3001101-0001X0PSAY

				AS3001101-0001X0IWAR
				AS3001101-0001X0IWAY
				AS3001101-0001X0PWAR
				AS3001101-0001X0PWAY
AS3004101-0001X	0I, 0P	SA, WA	R, Y	AS3004101-0001X0ISAR
				AS3004101-0001X0ISAY
				AS3004101-0001X0PSAR
				AS3004101-0001X0PSAY
				AS3004101-0001X0IWAR
				AS3004101-0001X0IWAY
				AS3004101-0001X0PWAR
				AS3004101-0001X0PWAY
AS3008101-0001X	0I, 0P	SA, WA	R, Y	AS3008101-0001X0ISAR
				AS3008101-0001X0ISAY
				AS3008101-0001X0PSAR
				AS3008101-0001X0PSAY
				AS3008101-0001X0IWAR
				AS3008101-0001X0IWAY
				AS3008101-0001X0PWAR
				AS3008101-0001X0PWAY
AS3016101-0001X	0I, 0P	SA, WA	R, Y	AS3016101-0001X0ISAR
				AS3016101-0001X0ISAY
				AS3016101-0001X0PSAR
				AS3016101-0001X0PSAY
				AS3016101-0001X0IWAR
				AS3016101-0001X0IWAY
				AS3016101-0001X0PWAR
				AS3016101-0001X0PWAY
Valid Combinations – 5MHz				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
AS1001101-0005X	0I, 0P	SA, WA	R, Y	AS1001101-0005X0ISAR
				AS1001101-0005X0ISAY
				AS1001101-0005X0PSAR
				AS1001101-0005X0PSAY
				AS1001101-0005X0IWAR
				AS1001101-0005X0IWAY
				AS1001101-0005X0PWAR
				AS1001101-0005X0PWAY
AS1004101-0005X	0I, 0P	SA, WA	R, Y	AS1004101-0005X0ISAR
				AS1004101-0005X0ISAY
				AS1004101-0005X0PSAR
				AS1004101-0005X0PSAY

				AS1004101-0005X0IWAR
				AS1004101-0005X0IWAY
				AS1004101-0005X0PWAR
				AS1004101-0005X0PWAY
AS1008101-0005X	0I, 0P	SA, WA	R, Y	AS1008101-0005X0ISAR
				AS1008101-0005X0ISAY
				AS1008101-0005X0PSAR
				AS1008101-0005X0PSAY
				AS1008101-0005X0IWAR
				AS1008101-0005X0IWAY
				AS1008101-0005X0PWAR
				AS1008101-0005X0PWAY
AS1016101-0005X	0I, 0P	SA, WA	R, Y	AS1016101-0005X0ISAR
				AS1016101-0005X0ISAY
				AS1016101-0005X0PSAR
				AS1016101-0005X0PSAY
				AS1016101-0005X0IWAR
				AS1016101-0005X0IWAY
				AS1016101-0005X0PWAR
				AS1016101-0005X0PWAY
AS3001101-0005X	0I, 0P	SA, WA	R, Y	AS3001101-0005X0ISAR
				AS3001101-0005X0ISAY
				AS3001101-0005X0PSAR
				AS3001101-0005X0PSAY
				AS3001101-0005X0IWAR
				AS3001101-0005X0IWAY
				AS3001101-0005X0PWAR
				AS3001101-0005X0PWAY
AS3004101-0005X	0I, 0P	SA, WA	R, Y	AS3004101-0005X0ISAR
				AS3004101-0005X0ISAY
				AS3004101-0005X0PSAR
				AS3004101-0005X0PSAY
				AS3004101-0005X0IWAR
				AS3004101-0005X0IWAY
				AS3004101-0005X0PWAR
				AS3004101-0005X0PWAY
AS3008101-0005X	0I, 0P	SA, WA	R, Y	AS3008101-0005X0ISAR
				AS3008101-0005X0ISAY
				AS3008101-0005X0PSAR
				AS3008101-0005X0PSAY
				AS3008101-0005X0IWAR
				AS3008101-0005X0IWAY
				AS3008101-0005X0PWAR

AS3016101-0005X	0I, 0P	SA, WA	R, Y	AS3008101-0005X0PWAY
				AS3016101-0005X0ISAR
				AS3016101-0005X0ISAY
				AS3016101-0005X0PSAR
				AS3016101-0005X0PSAY
				AS3016101-0005X0IWAR
				AS3016101-0005X0IWAY
				AS3016101-0005X0PWAR
Valid Combinations – 10MHz				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
AS1001101-0010X	0I, 0P	SA, WA	R, Y	AS1001101-0010X0ISAR
				AS1001101-0010X0ISAY
				AS1001101-0010X0PSAR
				AS1001101-0010X0PSAY
				AS1001101-0010X0IWAR
				AS1001101-0010X0IWAY
				AS1001101-0010X0PWAR
				AS1001101-0010X0PWAY
AS1004101-0010X	0I, 0P	SA, WA	R, Y	AS1004101-0010X0ISAR
				AS1004101-0010X0ISAY
				AS1004101-0010X0PSAR
				AS1004101-0010X0PSAY
				AS1004101-0010X0IWAR
				AS1004101-0010X0IWAY
				AS1004101-0010X0PWAR
				AS1004101-0010X0PWAY
AS1008101-0010X	0I, 0P	SA, WA	R, Y	AS1008101-0010X0ISAR
				AS1008101-0010X0ISAY
				AS1008101-0010X0PSAR
				AS1008101-0010X0PSAY
				AS1008101-0010X0IWAR
				AS1008101-0010X0IWAY
				AS1008101-0010X0PWAR
				AS1008101-0010X0PWAY
AS1016101-0010X	0I, 0P	SA, WA	R, Y	AS1016101-0010X0ISAR
				AS1016101-0010X0ISAY
				AS1016101-0010X0PSAR
				AS1016101-0010X0PSAY
				AS1016101-0010X0IWAR
				AS1016101-0010X0IWAY

AS3001101-0010X	0I, 0P	SA, WA	R, Y	AS1016101-0010X0PWAR
				AS1016101-0010X0PWAY
				AS3001101-0010X0ISAR
				AS3001101-0010X0ISAY
				AS3001101-0010X0PSAR
				AS3001101-0010X0PSAY
				AS3001101-0010X0IWAR
				AS3001101-0010X0IWAY
				AS3001101-0010X0PWAR
AS3001101-0010X0PWAY				
AS3004101-0010X	0I, 0P	SA, WA	R, Y	AS3004101-0010X0ISAR
				AS3004101-0010X0ISAY
				AS3004101-0010X0PSAR
				AS3004101-0010X0PSAY
				AS3004101-0010X0IWAR
				AS3004101-0010X0IWAY
				AS3004101-0010X0PWAR
				AS3004101-0010X0PWAY
AS3008101-0010X	0I, 0P	SA, WA	R, Y	AS3008101-0010X0ISAR
				AS3008101-0010X0ISAY
				AS3008101-0010X0PSAR
				AS3008101-0010X0PSAY
				AS3008101-0010X0IWAR
				AS3008101-0010X0IWAY
				AS3008101-0010X0PWAR
				AS3008101-0010X0PWAY
AS3016101-0010X	0I, 0P	SA, WA	R, Y	AS3016101-0010X0ISAR
				AS3016101-0010X0ISAY
				AS3016101-0010X0PSAR
				AS3016101-0010X0PSAY
				AS3016101-0010X0IWAR
				AS3016101-0010X0IWAY
				AS3016101-0010X0PWAR
				AS3016101-0010X0PWAY

Signal Description and Assignment

Figure 2: Device Pinout

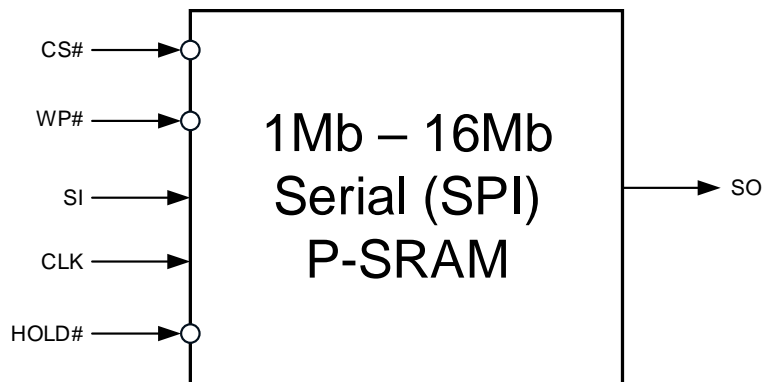


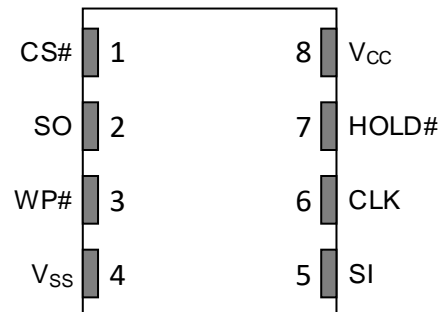
Table 2: Signal Description

Signal	Type	Description
CS#	Input	Chip Select: When CS# is driven High, the device will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS# Low enables the device, placing it in the active mode. After power-up, a falling edge on CS# is required prior to the start of any instructions.
WP#	Input	Write Protect: Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven.
CLK	Input	Clock: Provides the timing of the serial interface. Command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. The following two SPI clock modes are supported. <ul style="list-style-type: none"> • SPI Mode 0 (CPOL = 0, CPHA = 0) • SPI Mode 3 (CPOL = 1, CPHA = 1)
HOLD#	Input	Hold: Pauses serial communications with the device without deselecting or resetting the device. Outputs are tri-stated and inputs are ignored.
SI	Input	Serial Data Input: The unidirectional I/O transfers data into the device on the rising edge of the clock.
SO	Output	Serial Data Output: The unidirectional I/O transfers data out of the device on the falling edge of the clock.
V_{CC}	Supply	V_{CC}: Core and I/O power supply.
V_{SS}	Supply	V_{SS}: Core and I/O ground supply.

Package Options

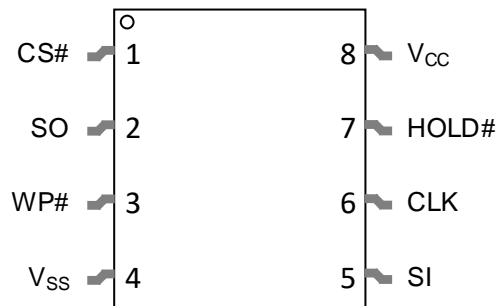
8-Pad WSON (Top View)

Figure 3: 8-Pad WSON



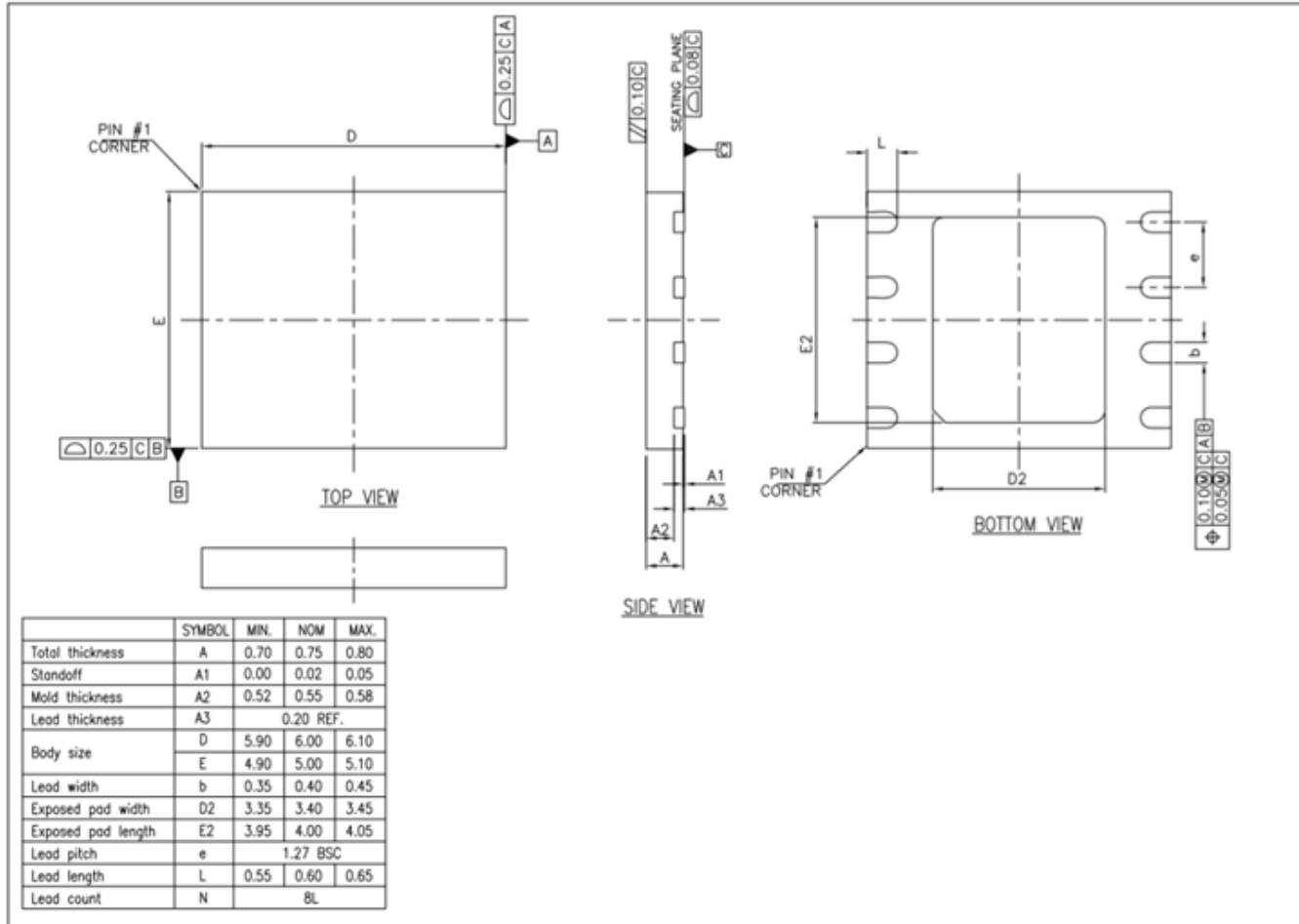
8-Pin SOIC (Top View)

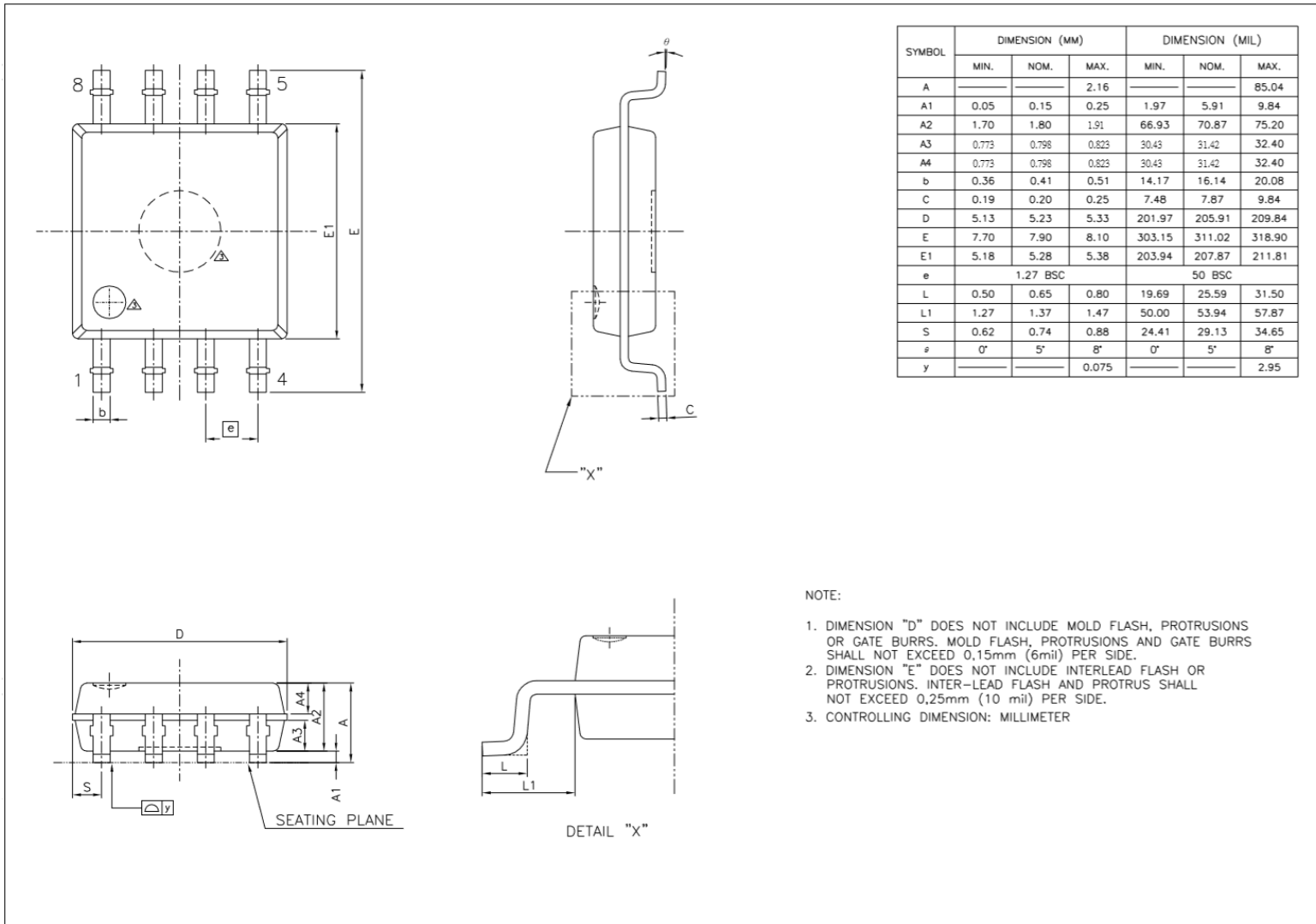
Figure 4: 8-Pin SOIC



Package Drawings

8-Pad WSON



8-Pin SOIC


Architecture

ASxxxx101 is an ultra-low power serial STT-MRAM device. It features a SPI-compatible bus interface and hardware/software based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB} .

ASxxxx101 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of CLK - CS# pin must be Low and the HOLD# pin must be High for the entire operation. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD# input and place ASxxxx101 in 'HOLD' state. After releasing the HOLD# pin, operation will resume from the point when the HOLD# was asserted.

ASxxxx101 has a 256-byte Augmented Storage Array which is independent from the main memory array. It is user programmable and can be locked against inadvertent writes.

The device offers both hardware and software based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the memory array.

Figure 5: Functional Block Diagram

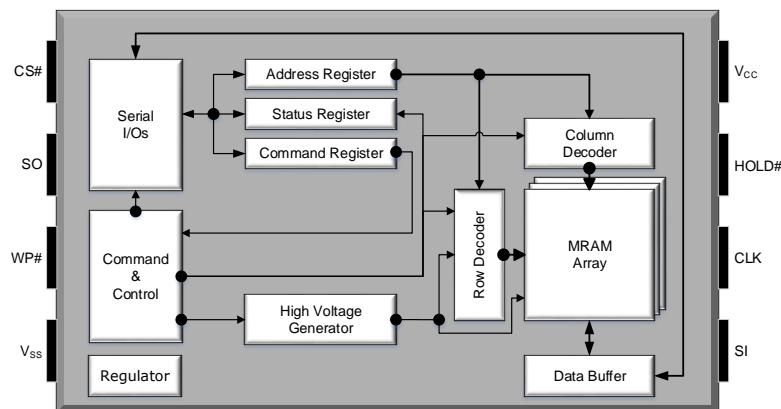


Table 3: Modes of Operation

Mode	CS#	Current	SI	SO	HOLD#
Standby	H	I_{SB}	Gated	Hi-Z	Gated
Active - Read	L	I_{READ}	Instruction	Dataout	H
Active - Write	L	I_{WRITE}	Instruction, Datain	Hi-Z	H
Hold	L	I_{READ}, I_{WRITE}	Not Gated	FD	L

Notes:

H: High (Logic '1')

L: Low (Logic '0')

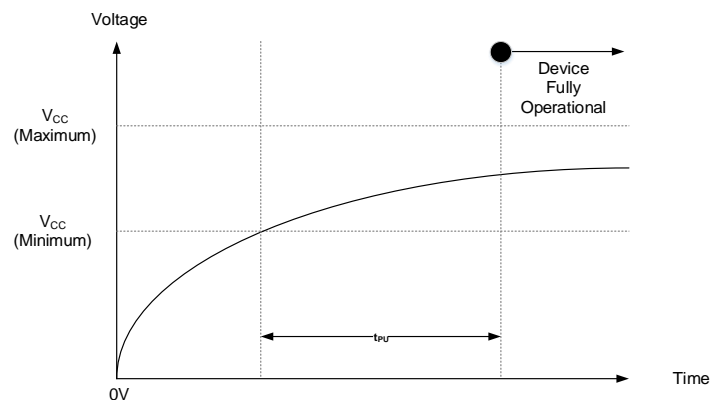
Hi-Z: High Impedance

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- Ramp up V_{CC} (R_{VR})
- CS# must follow V_{CC} during power-up (a 10K Ω pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- During initial Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences
- Upon Power-up, the device is in Standby mode

Figure 6: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- Ramp down V_{CC} (R_{VF})
- CS# must follow V_{CC} during power-down (a 10K Ω pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- The Power-up timing needs to be observed after V_{CC} goes above V_{CC} (minimum)

Figure 7: Power-Down Behavior

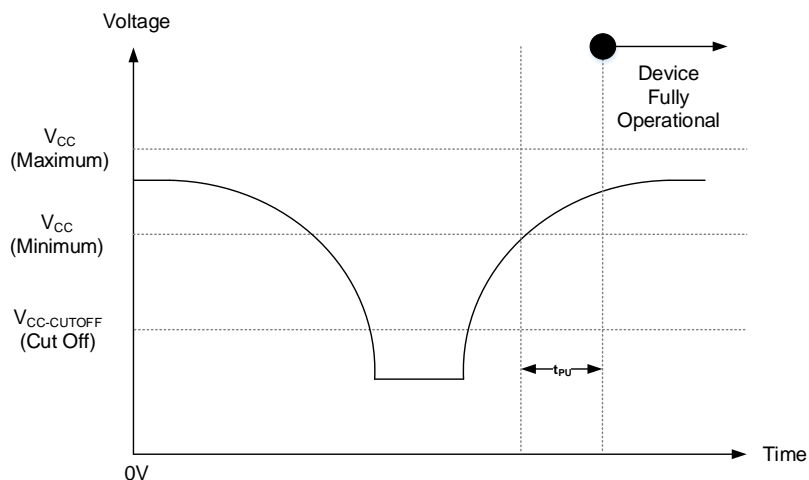


Table 4: Device Initialization Timing

Parameter	Symbol	Test Conditions	3.0V			Units
			Minimum	Typical	Maximum	
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R _{VR}	All operating voltages and temperatures	30	-	-	μs/V
V_{CC} Ramp Down Time	R _{VF}	All operating voltages and temperatures	20	-	-	μs/V
V_{CC} Power Up to First Instruction	t _{PU}	All operating voltages and temperatures	250	-	-	μs
V_{CC} Cutoff – Must Initialize Device	V _{CC-CUTOFF}	All operating voltages and temperatures	1.6	-	-	V

Table 5: Device Initialization Timing – 1.8V

Parameter	Symbol	Test Conditions	1.8V			Units
			Minimum	Typical	Maximum	
V_{CC} Range		All operating voltages and temperatures	1.71	-	2.0	V
V_{CC} Ramp Up Time	R _{VR}	All operating voltages and temperatures	30	-	-	μs/V
V_{CC} Ramp Down Time	R _{VF}	All operating voltages and temperatures	20	-	-	μs/V
V_{CC} Power Up to First Instruction	t _{PU}	All operating voltages and temperatures	250	-	-	μs
V_{CC} Cutoff – Must Initialize Device	V _{CC-CUTOFF}	All operating voltages and temperatures	1.6	-	-	V

Memory Map

Table 6: Memory Map

Density	Address Range	24-bit Address [23:0]	
1Mb	000000h – 01FFFFh	[23:17] – Logic '0'	[16:0] - Addressable
4Mb	000000h – 07FFFFh	[23:19] – Logic '0'	[18:0] - Addressable
8Mb	000000h – 0FFFFFFh	[23:20] – Logic '0'	[19:0] - Addressable
16Mb	000000h – 1FFFFFFh	[23:21] – Logic '0'	[20:0] - Addressable

Augmented Storage Array Map

Table 7: Augmented Storage Array Map

Density	Address Range	24-bit Address [23:0]	
1Mb	002000h – 0020FFh ¹	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable
4Mb	002000h – 0020FFh ¹	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable
8Mb	002000h – 0020FFh ¹	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable
16Mb	002000h – 0020FFh ¹	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

Table 8: Status Register

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	SNPEN	Serial Number Protection Enable/Disable	R/W	0	1: S/N Write protected - protection enabled 0: S/N Writable - protection disabled
SR[5]	TBPSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Enable/Disable	R	0	1: Write Operation Enabled 0: Write Operation Disabled
SR[0]	RSVD	Reserved	R	0	Reserved for future use

Table 9: Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb
0	0	0	None	None	None	None	None
0	0	1	Upper 1/64	01F800h – 01FFFFh	07E000h – 07FFFFh	0FC000h – 0FFFFFFh	1F8000h – 1FFFFFFh
0	1	0	Upper 1/32	01F000h – 01FFFFh	07C000h – 07FFFFh	0F8000h – 0FFFFFFh	1F0000h – 1FFFFFFh
0	1	1	Upper 1/16	01E000h – 01FFFFh	078000h – 07FFFFh	0F0000h – 0FFFFFFh	1E0000h – 1FFFFFFh
1	0	0	Upper 1/8	01C000h – 01FFFFh	070000h – 07FFFFh	0E0000h – 0FFFFFFh	1C0000h – 1FFFFFFh
1	0	1	Upper 1/4	018000h – 01FFFFh	060000h – 07FFFFh	0C0000h – 0FFFFFFh	180000h – 1FFFFFFh
1	1	0	Upper 1/2	010000h – 01FFFFh	040000h – 07FFFFh	080000h – 0FFFFFFh	1F0000h – 1FFFFFFh
1	1	1	All	00000h – 01FFFFh	00000h – 07FFFFh	00000h – 0FFFFFFh	00000h – 1FFFFFFh

Table 10: Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb
0	0	0	None	None	None	None	None
0	0	1	Lower 1/64	000000h – 0007FFh	000000h – 001FFFh	000000h – 003FFFh	000000h – 007FFFh
0	1	0	Lower 1/32	000000h – 00FFFFh	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh
0	1	1	Lower 1/16	000000h – 001FFFh	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh
1	0	0	Lower 1/8	000000h – 003FFFh	000000h – 00FFFFh	000000h – 01FFFFh	000000h – 03FFFFh
1	0	1	Lower 1/4	000000h – 007FFFh	000000h – 01FFFFh	000000h – 03FFFFh	000000h – 07FFFFh
1	1	0	Lower 1/2	000000h – 00FFFFh	000000h – 03FFFFh	000000h – 07FFFFh	000000h – 0FFFFFFh
1	1	1	All	000000h – 01FFFFh	000000h – 07FFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh

Table 11: Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status Register	Memory ¹ Array Protected Area	Memory ¹ Array Unprotected Area
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	Low	Protected	Protected	Unprotected
1	1	High	Unprotected	Protected	Unprotected

Notes:

High: Logic '1'

Low: Logic '0'

X: Don't Care – Can be Logic '0' or '1'

Protected: Write protected

Unprotected: Writable

1: Memory address range protection based on Block Protection Bits

Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 12: Device Identification Register – Read Only

Bits	Avalanche Manufacturer's ID	Device Configuration				
		Interface	Voltage	Temp	Density	Freq
ID[31:0]	ID[31:24]	ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1110 0110	0001-UPLP SPI	0001 - 3V	0000 - -40°C- 85°C	0001 - 1Mb	00000110 - 1MHz
		0010 - 1.8V	0001 - -40°C-105°C	0010 - 4Mb	00000111 - 5MHz
			0011 - 8Mb	00001000 - 10MHz	
			0100 - 16Mb	00001001 - 20MHz	

Serial Number Register (Read/Write)

Serial Number register is user writable.

Table 13: Serial Number Register – Read and Write

Bits	Name	Description	Read / Write	Default State ¹	Selection Options
SN[63:0]	SN	Serial Number Value	R/W	000000000000 0000h	Value stored is based on the customer

Unique Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

Table 14: Unique ID Register – Read Only

Bits	Name	Description	Read / Write	Selection Options
UID[63:0]	UID	Unique Identification Number Value	R	Value stored is written in the factory and is device specific

Instruction Set

Table 15: Instruction Set

#	Instruction Name	Command (Opcode)	1-0-0	1-0-1	1-1-1	Latency Cycles	Data Bytes	Address Bytes	Max. Frequency	Prerequisite
Control Instructions										
1	No Operation	NOOP - 00h	•					0	10MHz	
2	Write Enable	WREN- 06h	•					0	10MHz	
3	Write Disable	WRDI - 04h	•					0	10MHz	
4	Software Reset Enable	SRTE - 66h	•					0	10MHz	
5	Software Reset	SRST - 99h	•					0	10MHz	SRTE
Read Register Instructions										
6	Read Status Register ³	RDSR - 05h		•			1	0	10MHz	
7	Read Device ID ³	RDID - 9Fh		•			4	0	10MHz	
8	Read Unique ID ³	RUID - 4Ch		•			8	0	10MHz	
9	Read Serial Number Register ³	RDSN - C3h		•			8	0	10MHz	
Write Register Instructions										
10	Write Status Register	WRSR - 01h		•			1	0	10MHz	WREN
11	Write Serial Number Register	WRSN - C2h		•			8	0	10MHz	WREN
Read Memory Array Instructions										
12	Read Memory Array	READ - 03h			•		1 to ∞	3	10MHz	
13	Fast Read Memory Array ⁴	RDFT - 0Bh			•	•	1 to ∞	3	10MHz	
Write Memory Array Instructions										
14	Write Memory Array	WRTE - 02h			•		1 to ∞	3	10MHz	WREN
Augmented Storage Array Instructions										
15	Read Augmented Storage Array	RDAS - 4Bh			•		1 to 256	3 ²	10MHz	
16	Write Augmented Storage Array	WRAS - 42h			•		1 to 256	3 ²	10MHz	WREN

Notes:

1: The command code for an instruction is always transmitted on SI according to the SPI standard. However, an instruction may transmit address and data (send or receive) as well. The command-address-data column shows which of these three components the instruction contains. As an example, READ instruction has command, address, and data information: 1-1-1. On the other hand, SRST instruction only has command information: 1-0-0.

2: The augmented storage array is 256-Bytes in size.

3: Registers do not wrap data during reads. Reading beyond the specified number of bytes will yield indeterminate data.

4: Fast Read instruction requires 8 dummy CLK cycles after the address is entered and before the beginning of the read data. SI can be driven High or Low during the dummy CLK cycles.

5: The Status register needs to be re-initialized after a solder reflow process. Refer to the application note for the detailed description.

Instruction Description and Structures

All communication between a host and ASxxxx101 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from ASxxxx101. All command, address and data information is transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic '1').
- CLK marks the transfer of each bit.
- Each instructions starts out with an 8-bit command. The command selects the type of operation ASxxxx101 must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location. The address is always 24-bits wide. The address is transferred on the rising edges of CLK.
- The address bits are followed by data bits. Write data bits to ASxxxx101 are transferred on the rising edges of CLK. Read data bits from ASxxxx101 are transferred on the falling edges of CLK.
- Fast Read instruction (RDFT) requires 8 dummy CLK cycles after the address is entered and before the beginning of the read data. The dummy clock cycles are latency cycles. SI is ignored by ASxxxx101 during these dummy cycles.
- Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every write instruction. WREN bit can also be reset by executing the WRDI instruction.
- The entire memory array can be read from or written to using a single read or write instruction. After the starting address is entered, subsequent address are internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bit first.

Figure 8 to Figure 11 shows the description of instruction types supported.

Figure 8: Description of (1-0-0) Instruction Type

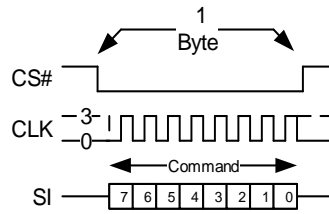


Figure 9: Description of (1-0-1) Instruction Type

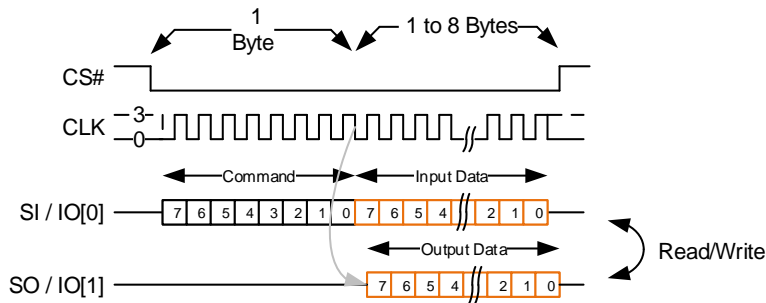


Figure 10: Description of (1-1-1) Instruction Type (No Latency)

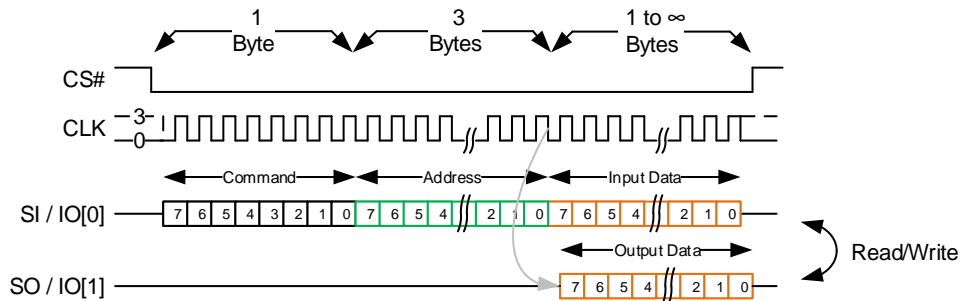
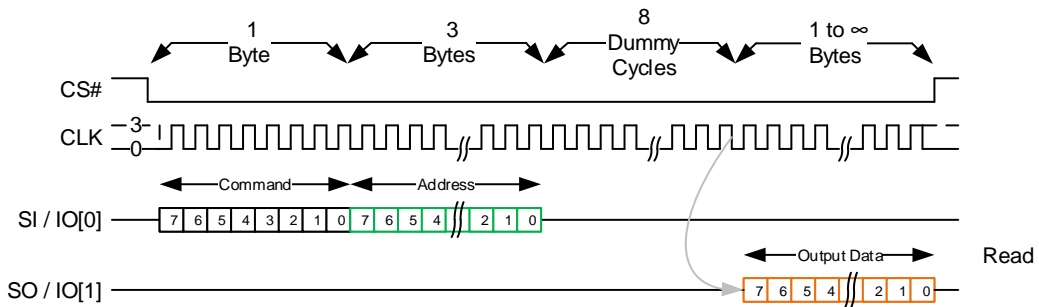


Figure 11: Description of (1-1-1) Instruction Type (With Latency)



Electrical Specifications

Table 16: Recommended Operating Conditions

Parameter / Condition	Minimum	Typical	Maximum	Units	
Operating Temperature	Industrial	-40.0	-	85.0	°C
	Industrial Plus	-40.0	-	105.0	°C
V_{CC} Supply Voltage (1.8V)	1.8V	1.71	1.8	2.0	V
V_{CC} Supply Voltage (3.0V)	3.0V	2.7	3.0	3.6	V
V_{SS} Supply Voltage		0.0	0.0	0.0	V

Table 17: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1MHz; V _{IN} = 3.0V	C _{IN}	6.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1MHz; V _{IN} = 3.0V	C _{INOUT}	8.0	pF

Table 18: Endurance & Data Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10 ¹⁴	cycles
Data Retention	RET	105°C	10	years
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

Table 19: 3.0V DC Characteristics

Parameter	Symbol	Test Conditions	3.0V Device (2.7V-3.6V)			Units
			Minimum	Typical	Maximum	
Read Current	I _{READ1}	V _{CC} = 3.6V, I _{OUT} =0mA, CLK=1MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	1.5	1.9	mA
Read Current	I _{READ2}	V _{CC} = 3.6V, I _{OUT} =0mA, CLK=5MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	2.0	2.5	mA
Read Current	I _{READ3}	V _{CC} = 3.6V, I _{OUT} =0mA, CLK=10MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	2.5	3.0	mA
Write Current	I _{WRITE1}	V _{CC} = 3.6V, I _{OUT} =0mA, CLK=1MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	10.0	12.0	mA
Write Current	I _{WRITE2}	V _{CC} = 3.6V, I _{OUT} =0mA, CLK=5MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	11.0	13.0	mA
Write Current	I _{WRITE3}	V _{CC} = 3.6V, I _{OUT} =0mA, CLK=10MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	12.0	14.0	mA
Standby Current Industrial (-40°C to 85°C)	I _{SB2}	V _{CC} = 3.6V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} , Temperature=85°C	-	2.5	9.0	µA
Standby Current Industrial Plus (-40°C to 105°C)	I _{SB3}	V _{CC} = 3.6V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} , Temperature=105°C	-	3.0	10.0	µA
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CC} (max)	-	-	±5.0	µA
Output Leakage Current	I _{LO}	V _{OUT} =0 to V _{CC} (max)	-	-	±5.0	µA
Input High Voltage	V _{IH}		0.7xV _{CC}	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL}		-0.3	-	0.3xV _{CC}	V
Output High Voltage Level	V _{OH}	I _{OH} = -100µA	V _{CC} -0.2	-	-	V
		I _{OH} = -1mA	2.4	-	-	V
Output Low Voltage Level	V _{OL}	I _{OL} = 150µA	-	-	0.2	V
		I _{OL} = 2mA	-	-	0.4	V

Table 20: 1.8V DC Characteristics

Parameter	Symbol	Test Conditions	1.8V Device (1.71V-2.0V)			Units
			Minimum	Typical	Maximum	
Read Current	I _{READ1}	V _{CC} = 2.0V, I _{OUT} =0mA, CLK=1MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	1.4	1.8	mA
Read Current	I _{READ2}	V _{CC} = 2.0V, I _{OUT} =0mA, CLK=5MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	1.7	2.2	mA
Read Current	I _{READ3}	V _{CC} = 2.0V, I _{OUT} =0mA, CLK=10MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	2.0	2.5	mA
Write Current	I _{WRITE1}	V _{CC} = 2.0V, I _{OUT} =0mA, CLK=1MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	8.0	9.0	mA
Write Current	I _{WRITE2}	V _{CC} = 2.0V, I _{OUT} =0mA, CLK=5MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	9.0	10.0	mA
Write Current	I _{WRITE3}	V _{CC} = 2.0V, I _{OUT} =0mA, CLK=10MHz (V _{IL} / V _{IH}), CS#= V _{IL} , SI= V _{IL} or V _{IH}	-	10.0	11.0	mA
Standby Current Industrial (-40°C to 85°C)	I _{SB2}	V _{CC} = 2.0V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} , Temperature=85°C	-	2.2	4.5	μA
Standby Current Industrial Plus (-40°C to 105°C)	I _{SB3}	V _{CC} = 2.0V, CLK=V _{CC} , CS#=V _{CC} , SI=V _{CC} , Temperature=105°C	-	2.5	5.0	μA
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CC} (max)	-	-	±5.0	μA
Output Leakage Current	I _{LO}	V _{OUT} =0 to V _{CC} (max)	-	-	±5.0	μA
Input High Voltage	V _{IH}		0.7xV _{CC}	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL}		-0.3	-	0.3xV _{CC}	V
Output High Voltage Level	V _{OH}	I _{OH} = -100μA	V _{CC} -0.2	-	-	V
		I _{OH} = -1mA	1.5	-	-	V
Output Low Voltage Level	V _{OL}	I _{OL} = 150μA	-	-	0.2	V
		I _{OL} = 2mA	-	-	0.4	V

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 21: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Junction Temperature	---	125	°C
Storage Temperature	-55 to 150		°C
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ 2000 V		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ 500 V		V
Latch-Up (I-test) JESD78	≥ 100 mA		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

Table 22: AC Test Conditions

Parameter	Value
Input Pulse Levels	0.0V to V _{CC}
Input Rise and Fall Times	3.0ns
Input and Output Measurement Timing Levels	V _{CC} /2
Output Load	CL = 30.0pF

CS# Operation & Timing

Figure 12: CS# Operation & Timing

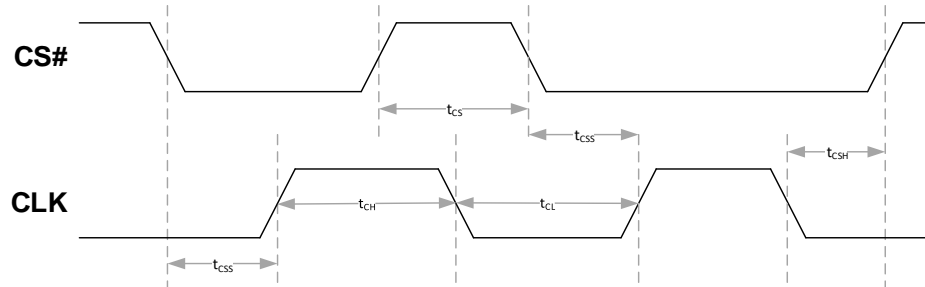


Table 23: CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1.0	10.0	MHz
Clock Low Time	t_{CL}	11.0	-	ns
Clock High Time	t_{CH}	11.0	-	ns
Chip Deselect Time after Status Register Write	t_{CS1}	3.0	-	μ s
Chip Deselect Time after SN Register Write	t_{CS2}	10.0	-	μ s
Chip Deselect Time after Memory Array Read / Write	t_{CS3}	40.0	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5.0	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	5.0	-	ns

Notes:

Power supplies must be stable

Command, Address and Data Input Operation & Timing

Figure 13: Command, Address and Data Input Operation & Timing

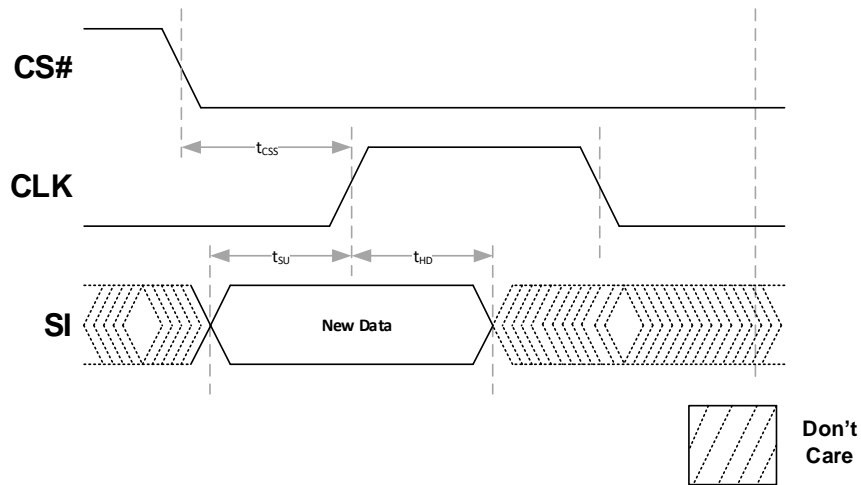


Table 24: Command, Address and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	5.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	5.0	-	ns

Notes:

Power supplies must be stable

Data Output Operation & Timing

Figure 14: Data Output Operation & Timing

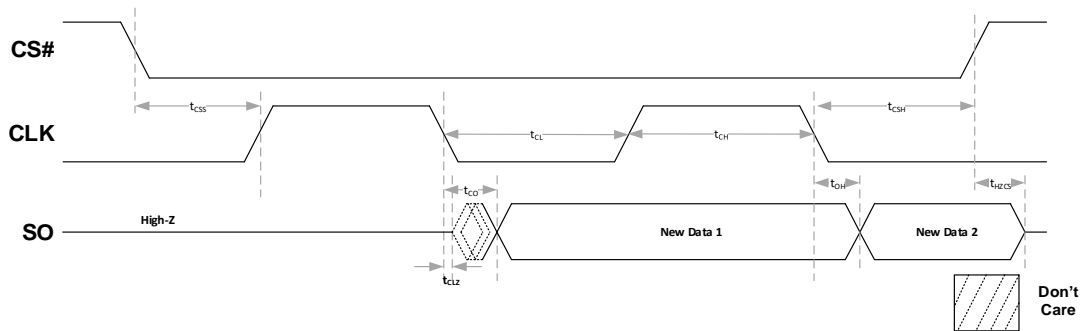


Table 25: Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	9.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	12	ns

Notes:

Power supplies must be stable

WP# Operation & Timing

Figure 15: WP# Operation & Timing

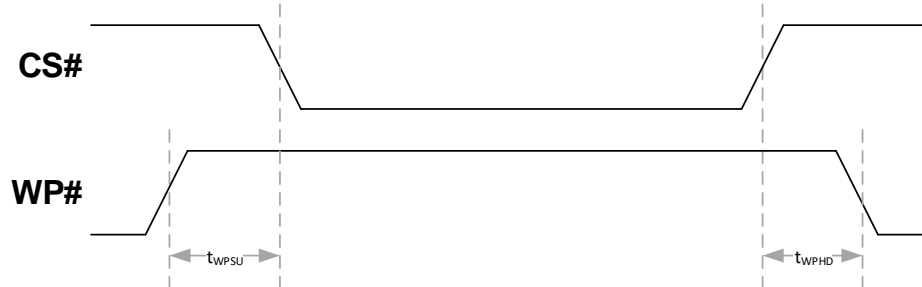


Table 26: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	t_{WPSU}	20	-	ns
WP# Hold Time (w.r.t CS#)	t_{WPHD}	20	-	ns

Notes:

Power supplies must be stable

HOLD# Operation & Timing

Figure 16: HOLD# Operation & Timing

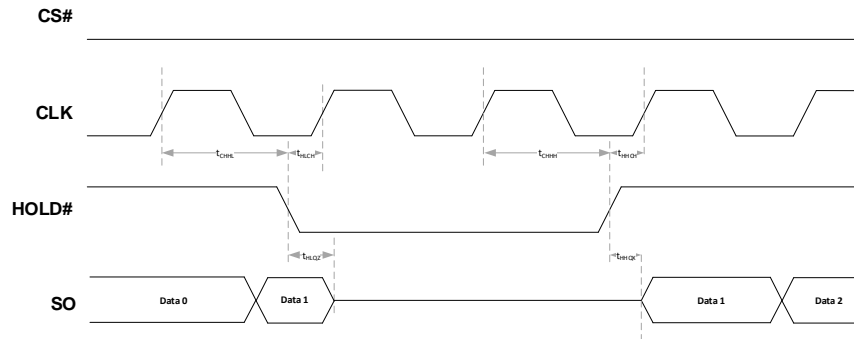


Table 27: HOLD# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
HOLD# Active Setup Time (w.r.t CLK)	t_{CHHL}	10	-	ns
HOLD# Active Hold Time (w.r.t CLK)	t_{HLCH}	10	-	ns
HOLD# Inactive Setup Time (w.r.t CLK)	t_{CHHH}	10	-	ns
HOLD# Inactive Hold Time (w.r.t CLK)	t_{HHCH}	10	-	ns
HOLD# to Output Low-Z (Active)	t_{HHQX}	-	20	ns
HOLD# to Output High-Z	t_{HLQZ}	-	20	ns

Notes:

Power supplies must be stable

Thermal Resistance

Table 28: Thermal Resistance Specifications

Parameter	Description	Test Conditions	8-pad WSON	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	43.67	53.59	°C/W
θ_{JC}	Thermal resistance (junction to case)		18.54	4.29	

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

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Revision History

Revision	Date	Change Summary
REV J	04/17/2020	Added 1.8V DC Characteristics Table 20. Updated 3.0V DC Characteristics Table 19. Added ESD and Latch-up specifications. Added junction and storage temperature specifications. Combined magnetic immunity and ESD tables.
REV K	06/03/2020	Updated Icc read, write and standby values. Corrected Ordering options. General cleanup.
REV L	09/09/2020	Added detailed Data Retention specifications on page 25. Added Thermal Resistance specifications on page 34