Parallel Persistent SRAM Memory

(AS3001316, AS3004316, AS3008316, AS3016316, AS3032316, AS3064316)

Features

- Interface
  - Parallel Asynchronous x16
- Technology
  - 40nm pMTJ STT-MRAM
    - Virtually unlimited Endurance and Data Retention (see Endurance and Data Retention on page 24)
- Density
  - 1Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
- Operating Temperature Range
  - Industrial: -40°C to 85°C
  - Industrial Plus: -40°C to 105°C
- RoHS & REACH Compliant
- Packages
  - 44-pin TSOP (10mm x 18mm)
  - 54-pin TSOP (10mm x 22mm)
  - 48-ball FBGA (10mm x 10mm)
- Memory Array Organization
  - 1Mbit
    - 65,536 x 16
  - 4Mbit
    - 262,144 x 16
  - 8Mbit
    - 524,288 x 16
  - 16Mbit
    - 1,048,576 x 16
  - 32Mbit
    - 2,097,152 x 16
  - 64Mbit
    - 4,194,304 x 16

Performance

Device Operation	Typical Values	Units
Read Cycle Time	35.0 (minimum)	ns
Write Cycle Time	35.0 (minimum)	ns
Standby Current	1.7 (typical)*	mA
Read Current	12.0 (typical)	mA
Write Current	20.0 (typical)	mA

*Number shown is for 16Mb device

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General Description

AS3xxx316 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 1Mbit to 32Mbit. MRAM technology is analogous to Flash technology with SRAM compatible 35ns/35ns and 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually unlimited endurance and data retention, high performance and scalable memory technology.

AS3xxx316 is available in small footprint 54-pin TSOP (10mm x 22mm) and 48-Ball FBGA (10mm x 10mm) packages supporting densities ranging from 1Mb to 32Mb. Densities of 1Mb and 4Mb are also available in a small footprint 44-pin TSOP (10mm x 18mm). These packages are compatible with similar low-power volatile and non-volatile products.

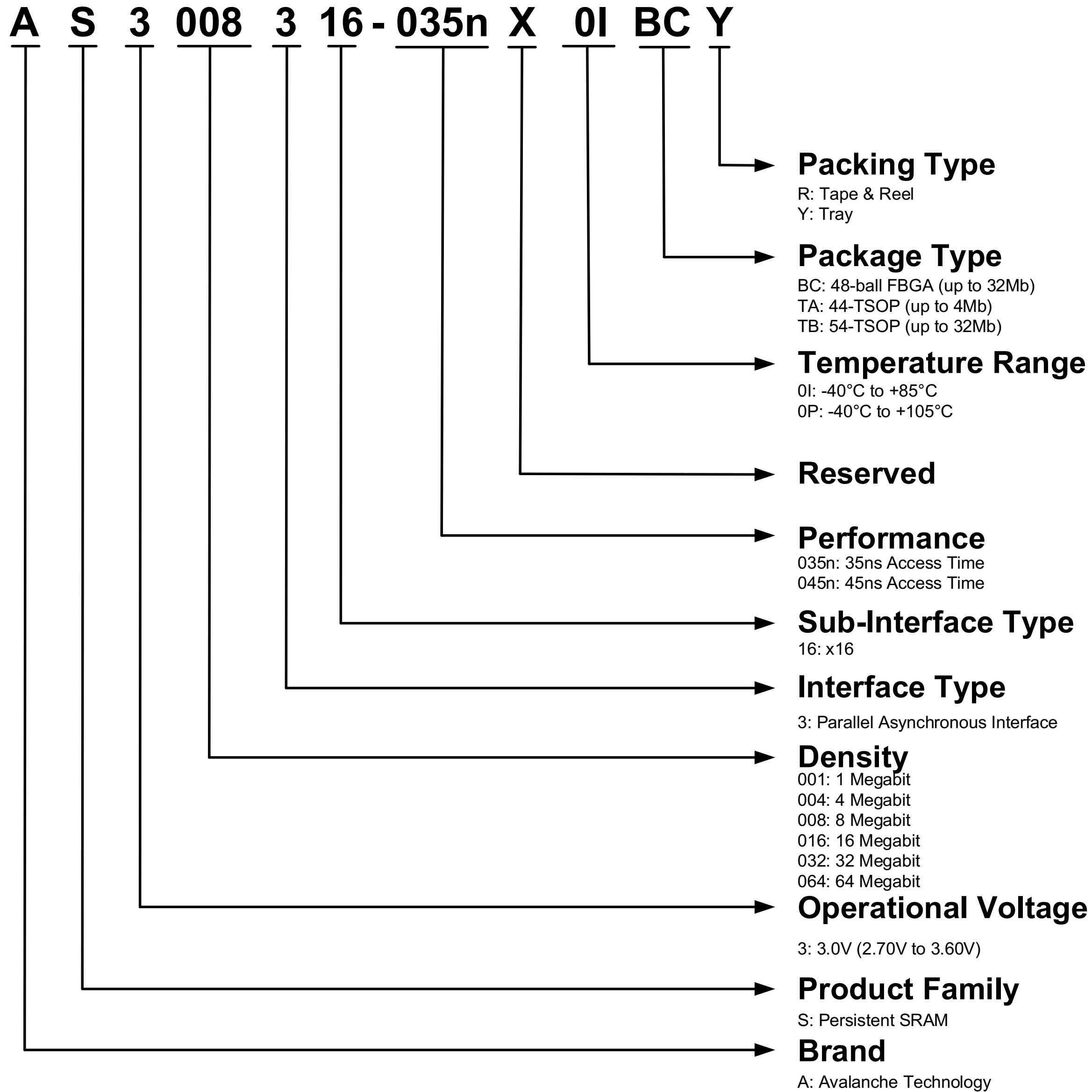
AS3xxx316 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

AS3064316 (64Mb density) is offered with industrial (-40°C to 85°C) operating temperature ranges in a 48-Ball FBGA (10mm x 10mm) package.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Part Number Ordering System



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2: Valid Combinations List

Valid Combinations – 35ns				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS3001316-035nX	0I, 0P	BC, TA, TB	R, Y	AS3001316-035nX0IBCR
				AS3001316-035nX0IBCY
				AS3001316-035nX0ITAR
				AS3001316-035nX0ITAY
				AS3001316-035nX0ITBR
				AS3001316-035nX0ITBY
				AS3001316-035nX0PBCR
				AS3001316-035nX0PBCY
				AS3001316-035nX0PTAR
				AS3001316-035nX0PTAY
				AS3001316-035nX0PTBR
				AS3001316-035nX0PTBY
AS3004316-035nX	0I, 0P	BC, TA, TB	R, Y	AS3004316-035nX0IBCR
				AS3004316-035nX0IBCY
				AS3004316-035nX0ITAR
				AS3004316-035nX0ITAY
				AS3004316-035nX0ITBR
				AS3004316-035nX0ITBY
				AS3004316-035nX0PBCR
				AS3004316-035nX0PBCY
				AS3004316-035nX0PTAR
				AS3004316-035nX0PTAY
				AS3004316-035nX0PTBR
				AS3004316-035nX0PTBY
AS3008316-035nX	0I, 0P	BC, TB	R, Y	AS3008316-035nX0IBCR
				AS3008316-035nX0IBCY
				AS3008316-035nX0ITBR
				AS3008316-035nX0ITBY
				AS3008316-035nX0PBCR
				AS3008316-035nX0PBCY
				AS3008316-035nX0PTBR
				AS3008316-035nX0PTBY
AS3016316-035nX	0I, 0P	BC, TB	R, Y	AS3016316-035nX0IBCR
				AS3016316-035nX0IBCY

Valid Combinations – 35ns				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
				AS3016316-035nX0ITBR
				AS3016316-035nX0ITBY
				AS3016316-035nX0PBCR
				AS3016316-035nX0PBCY
				AS3016316-035nX0PTBR
				AS3016316-035nX0PTBY
AS3032316-035nX	0I, 0P	BC, TB	R, Y	AS3032316-035nX0IBCR
				AS3032316-035nX0IBCY
				AS3032316-035nX0ITBR
				AS3032316-035nX0ITBY
				AS3032316-035nX0PBCR
				AS3032316-035nX0PBCY
				AS3032316-035nX0PTBR
				AS3032316-035nX0PTBY

Valid Combinations – 45ns				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS3001316-045nX	0I, 0P	BC, TA, TB	R, Y	AS3001316-045nX0IBCR
				AS3001316-045nX0IBCY
				AS3001316-045nX0ITAR
				AS3001316-045nX0ITAY
				AS3001316-045nX0ITBR
				AS3001316-045nX0ITBY
				AS3001316-045nX0PBCR
				AS3001316-045nX0PBCY
				AS3001316-045nX0PTAR
				AS3001316-045nX0PTAY
				AS3001316-045nX0PTBR
				AS3001316-045nX0PTBY
AS3004316-045nX	0I, 0P	BC, TA, TB	R, Y	AS3004316-045nX0IBCR
				AS3004316-045nX0IBCY
				AS3004316-045nX0ITAR
				AS3004316-045nX0ITAY
				AS3004316-045nX0ITBR
				AS3004316-045nX0ITBY
				AS3004316-045nX0PBCR
				AS3004316-045nX0PBCY

Valid Combinations – 45ns				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
				AS3004316-045nX0PTAR
				AS3004316-045nX0PTAY
				AS3004316-045nX0PTBR
				AS3004316-045nX0PTBY
AS3008316-045nX	0I, 0P	BC, TB	R, Y	AS3008316-045nX0IBCR
				AS3008316-045nX0IBCY
				AS3008316-045nX0ITBR
				AS3008316-045nX0ITBY
				AS3008316-045nX0PBCR
				AS3008316-045nX0PBCY
				AS3008316-045nX0PTBR
				AS3008316-045nX0PTBY
AS3016316-045nX	0I, 0P	BC, TB	R, Y	AS3016316-045nX0IBCR
				AS3016316-045nX0IBCY
				AS3016316-045nX0ITBR
				AS3016316-045nX0ITBY
				AS3016316-045nX0PBCR
				AS3016316-045nX0PBCY
				AS3016316-045nX0PTBR
				AS3016316-045nX0PTBY
AS3032316-045nX	0I, 0P	BC, TB	R, Y	AS3032316-045nX0IBCR
				AS3032316-045nX0IBCY
				AS3032316-045nX0ITBR
				AS3032316-045nX0ITBY
				AS3032316-045nX0PBCR
				AS3032316-045nX0PBCY
				AS3032316-045nX0PTBR
				AS3032316-045nX0PTBY
AS3064316-045nX	0I	BC	Y	AS3064316-045nX0IBCY

Signal Description and Assignment

Figure 2: Device Pinout

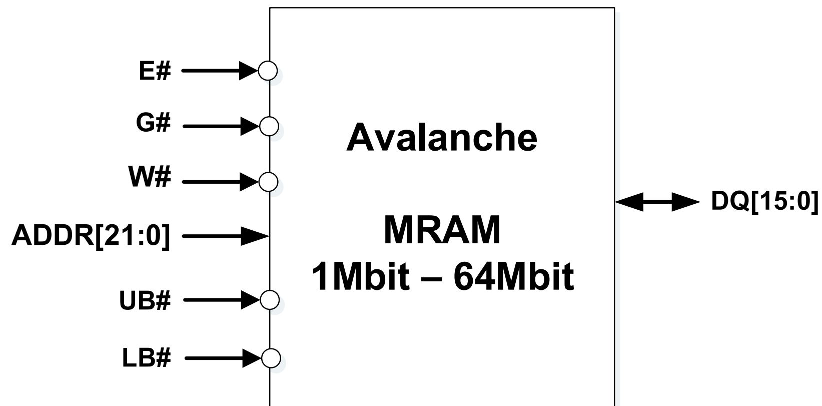
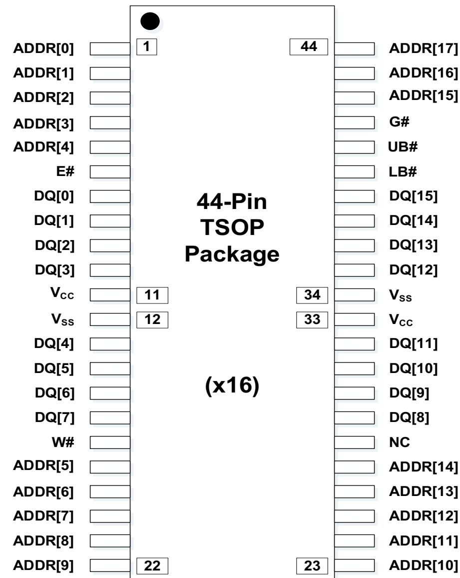


Table 3: Signal Description

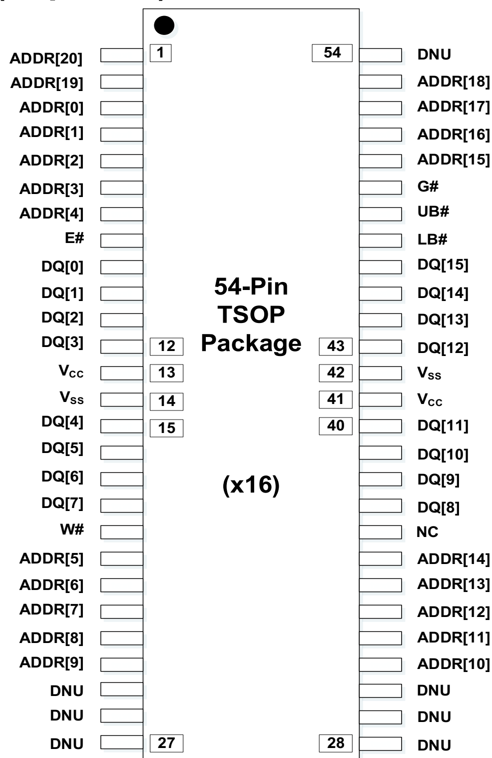
Signal	Type	Description
E#	Input	**Chip enable:** Enables or disables the MRAM.
G#	Input	**Output enable:** Enables the output drivers in bidirectional data transfer I/Os.
W#	Input	**Write enable:** Transfers serial data from the host system to the MRAM when Low (Logic '0').Transfers serial data from the MRAM to the host system when High (Logic '1').
UB#	Input	**Upper Byte Enable:** Enables or disables DQ[15:8].
LB#	Input	**Lower Byte Enable:** Enables or disables DQ[7:0].
ADDR[21:0]	Input	**Address:** I/Os for address transfer. 01M: ADDR[15:0] – 16 Address pins for 01M devices. 04M: ADDR[17:0] – 18 Address pins for 04M devices. 08M: ADDR[18:0] – 19 Address pins for 08M devices. 16M: ADDR[19:0] – 20 Address pins for 16M devices. 32M: ADDR[20:0] – 21 Address pins for 32M devices. 64M: ADDR[21:0] – 22 Address pins for 64M devices.
DQ[15:0]	Input / Output	**Data inputs/outputs:** The bidirectional I/Os transfer data.
V_{CC}	Supply	**V_{CC}:** Core and I/O power supply.
V_{SS}	Supply	**V_{SS}:** Core and I/O ground supply.
NC		**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU		**Do not use:** DNUs must be left unconnected.

Package Options

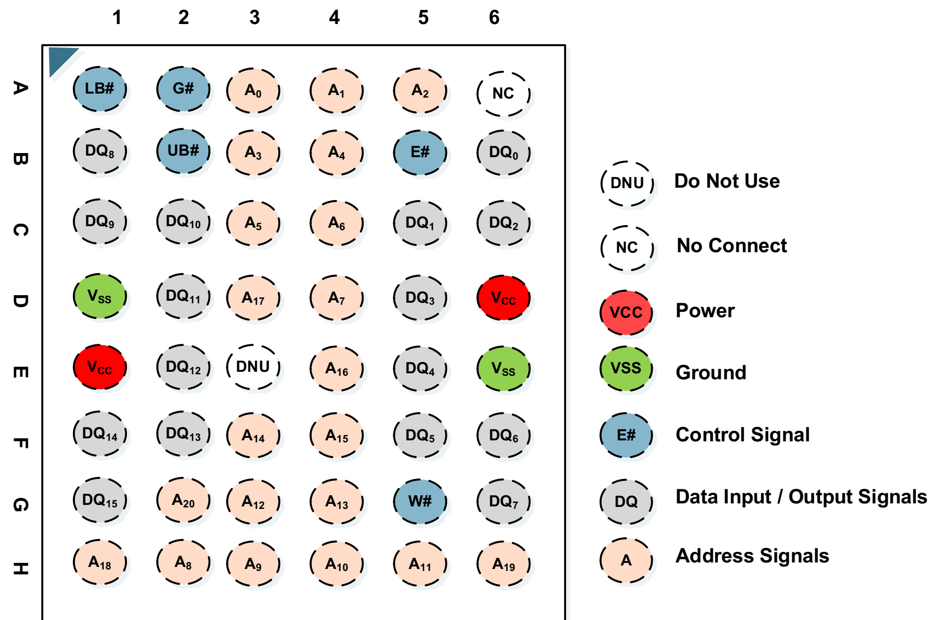
44-Pin TSOP (1-4Mb) (Top View)



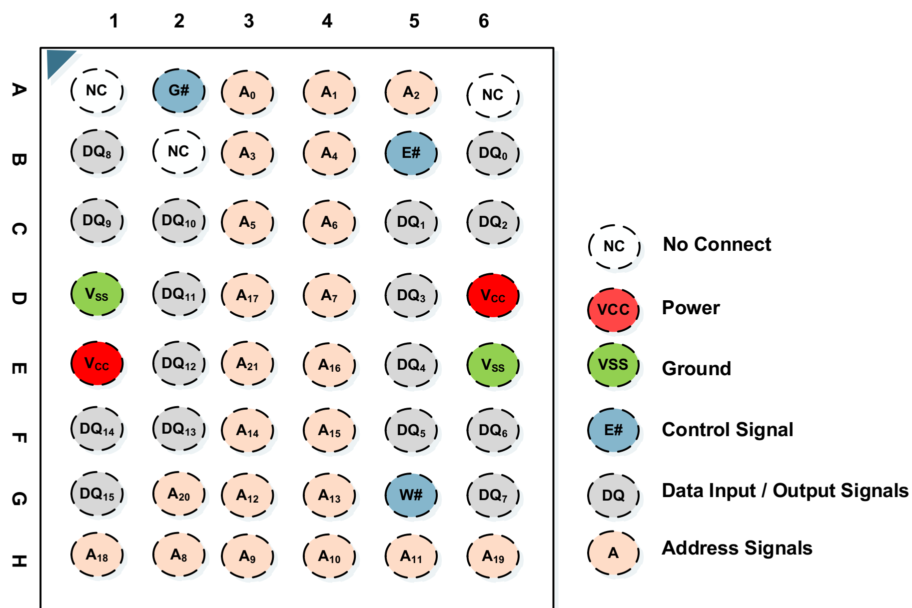
54-Pin TSOP (1-32Mb) (Top View)



48-Ball FBGA (1-32Mb) (Balls Down, Top View)

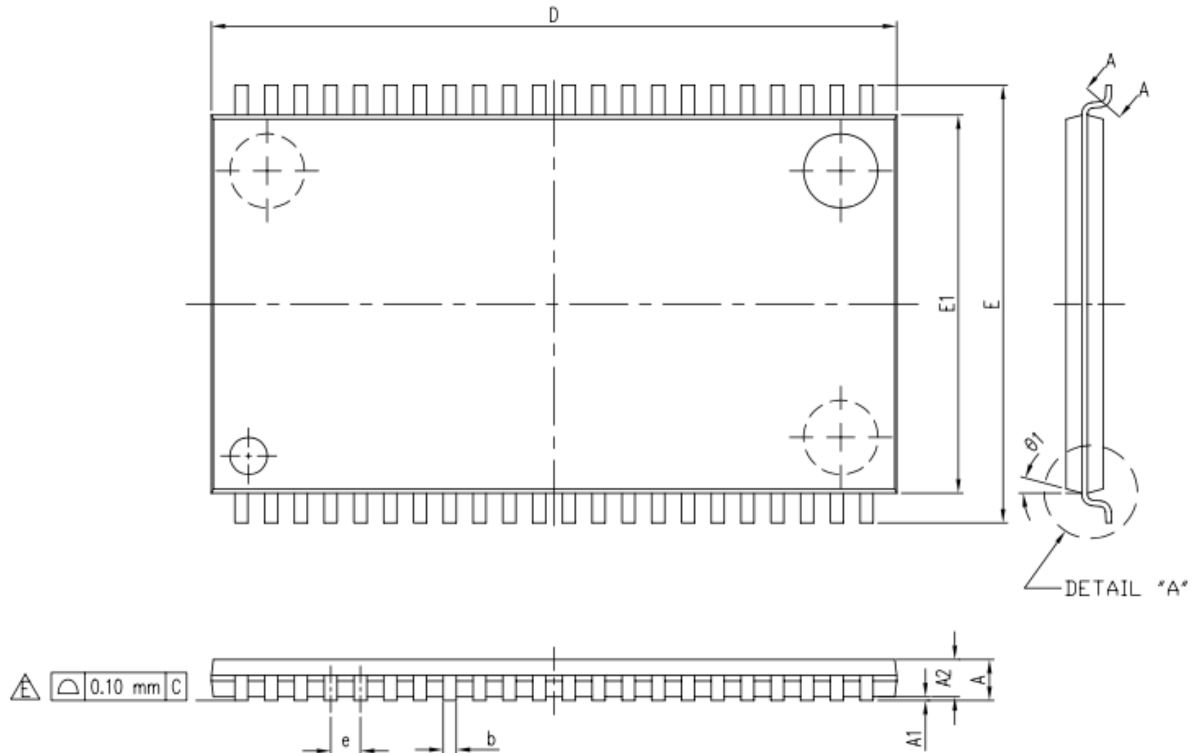


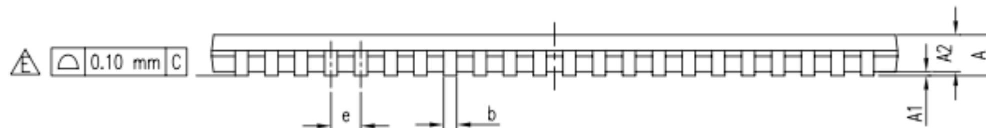
48-Ball FBGA (64Mb) (Balls Down, Top View)

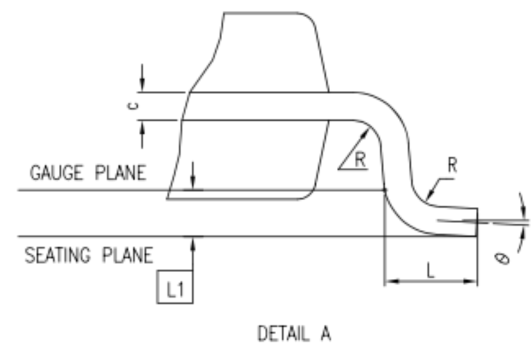


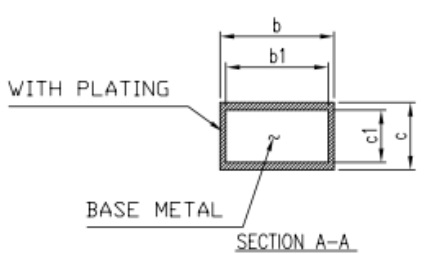
Package Drawings

44-Pin TSOP





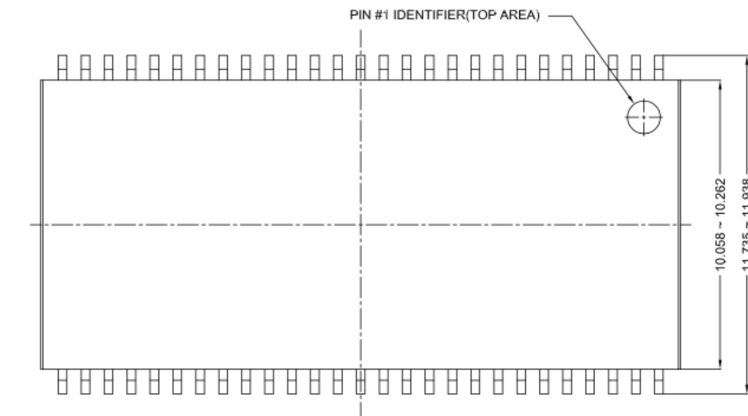




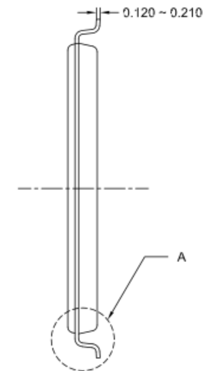
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
(A) b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12		0.21	0.005		0.008
(A) c1	0.12	0.15	0.16	0.005	0.006	0.006
e	0.80 BASIC			0.031 BASIC		
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BASIC			0.010 BASIC		
R	0.12		0.25	0.005		0.010
(B) θ	0		8	0		8
θ1	10	15	20	10	15	20
(C) N	44L					
JEDEC	MO-133(BA)					

NOTE : DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.
D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

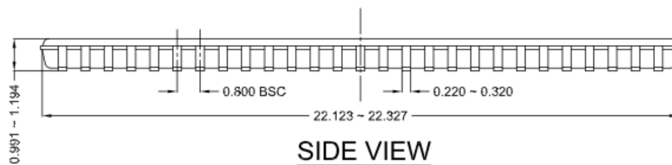
54-Pin TSOP



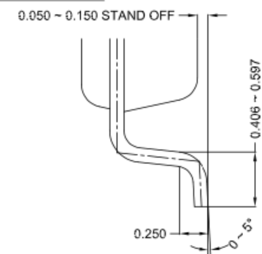
TOP VIEW



SIDE VIEW



SIDE VIEW

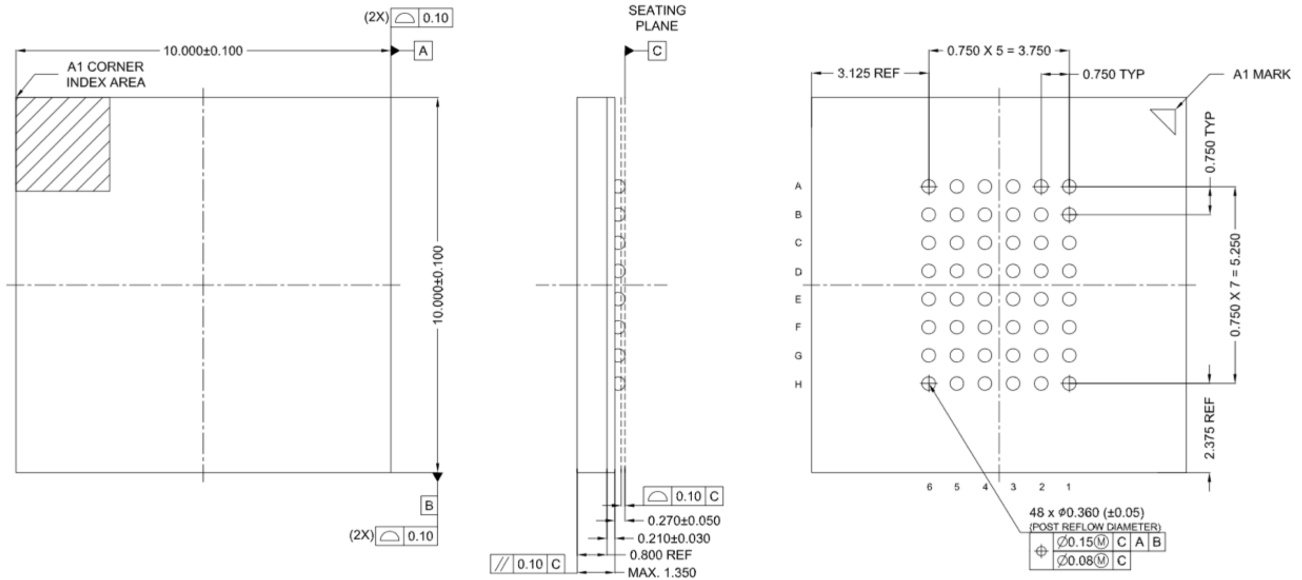


DETAIL "A"

(Unit : mm)

		COMMON DIMENSIONS		
		MIN	NOM	MAX
Package		54TSOP		
Body size	X	-	-	-
	Y	11.735	-	11.938
Mold size	X	22.123	-	22.327
	Y	10.058	-	10.262
Lead Pitch		0.800 BSC		
Total Thickness		0.991	-	1.194
Lead Frame Thickness		0.120	-	0.210
Stand Off		0.050	-	0.150
LEAD Width		0.220	-	0.320

48-Ball FBGA



(Unit : mm)

		COMMON DIMENSIONS		
		MIN	NOM	MAX
Package			48 FBGA	
Body size	X	9.900	10.000	10.100
	Y	9.900	10.000	10.100
Ball Pitch			0.750	
Total Thickness				1.350
Mold Thickness			0.800 Ref.	
Substrate Thickness		0.180	0.210	0.240
Ball Diameter (Raw Ball Size)			0.350	
Stand Off		0.220	0.270	0.320
Ball Width (Post Reflow size)		0.310	0.360	0.410
Package Edge Tolerance			0.100	
Mold Parallelism			0.100	
Coplanarity			0.100	
Ball Offset (Package)			0.150	
Ball Offset (Ball)			0.050	
Ball Count			63	
Edge Ball Center to Center	X		3.750	
	Y		5.250	

Architecture

AS3xxx316 is a high performance MRAM device. Writing to and reading from the device as follows:

To write to the device, bring Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[15]) to be written into the memory location specified by the address pins ADDR[0] through ADDR[20] (54-pin TSOP and 48-ball FBGA) and ADDR[0] through ADDR[17] (44-pin TSOP).

To read from the device, bring Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins ADDR[0] through ADDR[20] (54-pin TSOP and 48-ball FBGA) and ADDR[0] through ADDR[17] (44-pin TSOP) to appear on I/O pins (DQ[0] to DQ[15]).

Figure 3: Functional Block Diagram

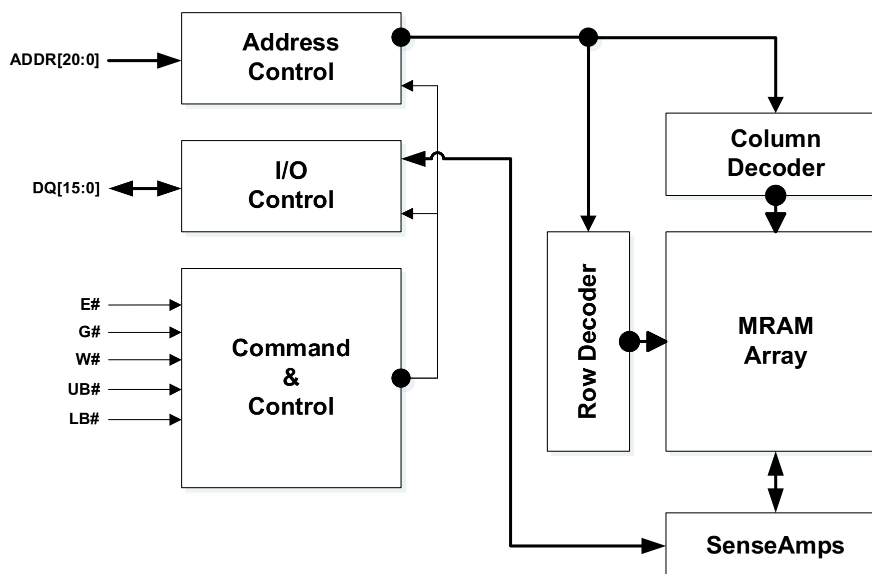


Table 4: Modes of Operation

Mode	E#	G#	W#	UB#[1]	LB#[1]	Current	DQ[15:8]	DQ[7:0]
Not Selected	H	X	X	X	X	I_{SB}	Hi-Z	Hi-Z
Output Disabled	L	H	H	X	X	I_{READ}	Hi-Z	Hi-Z
Output Disabled	L	X	X	H	H	I_{READ}	Hi-Z	Hi-Z
Read Upper Byte	L	L	H	L	H	I_{READ}	Dataout	Hi-Z
Read Lower Byte	L	L	H	H	L	I_{READ}	Hi-Z	Dataout
Read Word	L	L	H	L	L	I_{READ}	Dataout	Dataout
Write Upper Byte	L	X	L	L	H	I_{WRITE}	Datain	Hi-Z
Write Lower Byte	L	X	L	H	L	I_{WRITE}	Hi-Z	Datain
Write Word	L	X	L	L	L	I_{WRITE}	Datain	Datain

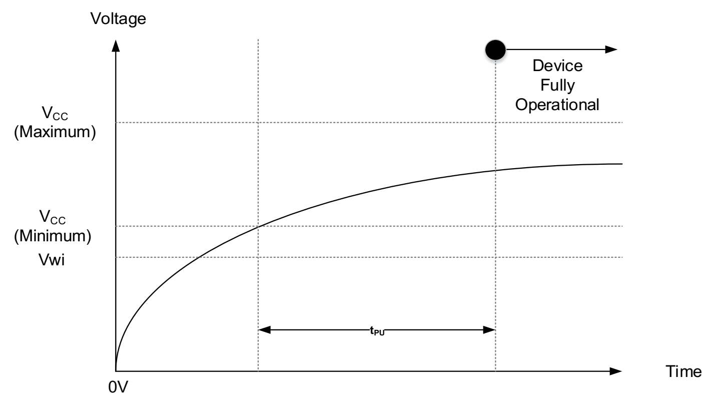
Notes:
H: High (Logic '1') X: Don't Care
L: Low (Logic '0') Hi-Z: High Impedance
1: UB# and LB# functionality is not available in the 64Mb device.

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- E#, W#, G# must follow V_{CC} during power-up

Figure 4: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- E#, W#, G# must follow V_{CC} during power-down
- During power loss or brownout, where Vcc goes below Vwi, read/write operations are prohibited. The power-up timing needs to be observed after Vcc goes above Vcc (minimum)

Figure 5: Power-Down Behavior

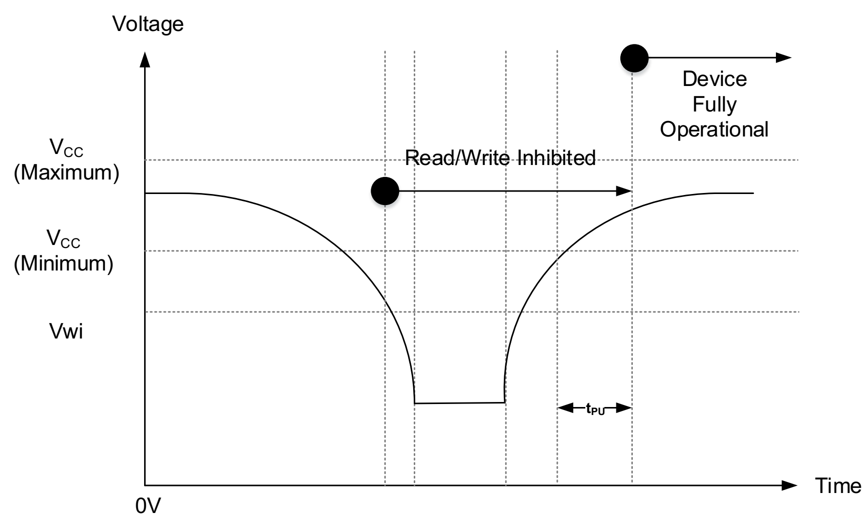


Table 6: Device Initialization Timing – 3.0V

Parameter	Symbol	Test Conditions	3.0V			
			Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Power Up to First Instruction	t_{PU}	All operating voltages and temperatures	-	-	1	ms

Electrical Specifications

Table 7: Recommended Operating Conditions

Parameter / Condition		Minimum	Typical	Maximum	Units
	Industrial	-40.0	-	85.0	°C
	Industrial Plus	-40.0	-	105.0	°C
V_{CC} Supply Voltage	3.0V	2.7	3.0	3.6	V
V_{SS} Supply Voltage		0.0	0.0	0.0	V
Vwi Write Inhibit Voltage		2.1	2.3	2.5	V

Table 8: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V Density = 1Mb – 16Mb	C_{IN}	10.0	pF
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V Density = 32Mb		20.0	
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V Density = 64Mb		40.0	
Input / Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V Density = 1Mb – 16Mb	C_{INOUT}	10.0	pF
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V Density = 32Mb		20.0	
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V Density = 64Mb		20.0	

Table 9: DC Characteristics

Parameter	Symbol	Test Conditions		3.0V Device (2.7V-3.6V)			Units
				Minimum	Typical	Maximum	
Read Current	I_{READ}	V_{CC} (max), I_{OUT}=0mA	1Mb – 32Mb	-	12.0	30.0	mA
			64Mb		24.0	60.0	
Write Current	I_{WRITE}	V_{CC} (max)	1Mb – 32Mb	-	20.0	30.0	mA
			64Mb		40.0	60.0	
Standby Current Industrial (-40°C to 85°C)	I_{SB}	E#=V_{IH}, V_{CC} (max)	1Mb-16Mb	-	1.5	2.5	mA
			32Mb		3.0	5.0	
			64Mb		6.0	10.0	
Standby Current Industrial Extended (-40°C to 105°C)	I_{SB}	E#=V_{IH}, V_{CC} (max)	1Mb-16Mb	-	1.7	3.5	mA
			32Mb		3.4	7.0	
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.8xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.5	-	0.2xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -1.6mA		V_{CC}-0.5	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1.6mA		-	-	0.4	V

Table 10: Magnetic Immunity Characteristics

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	H_{max_write}	24000	A/m
Magnetic Field During Read	H_{max_read}	24000	A/m

Table 11: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	5ns
Input and output measurement timing levels	$V_{CC}/2$
Output Load	CL = 30pF

Write Operation

Figure 7: Write Operation (W# Controlled)

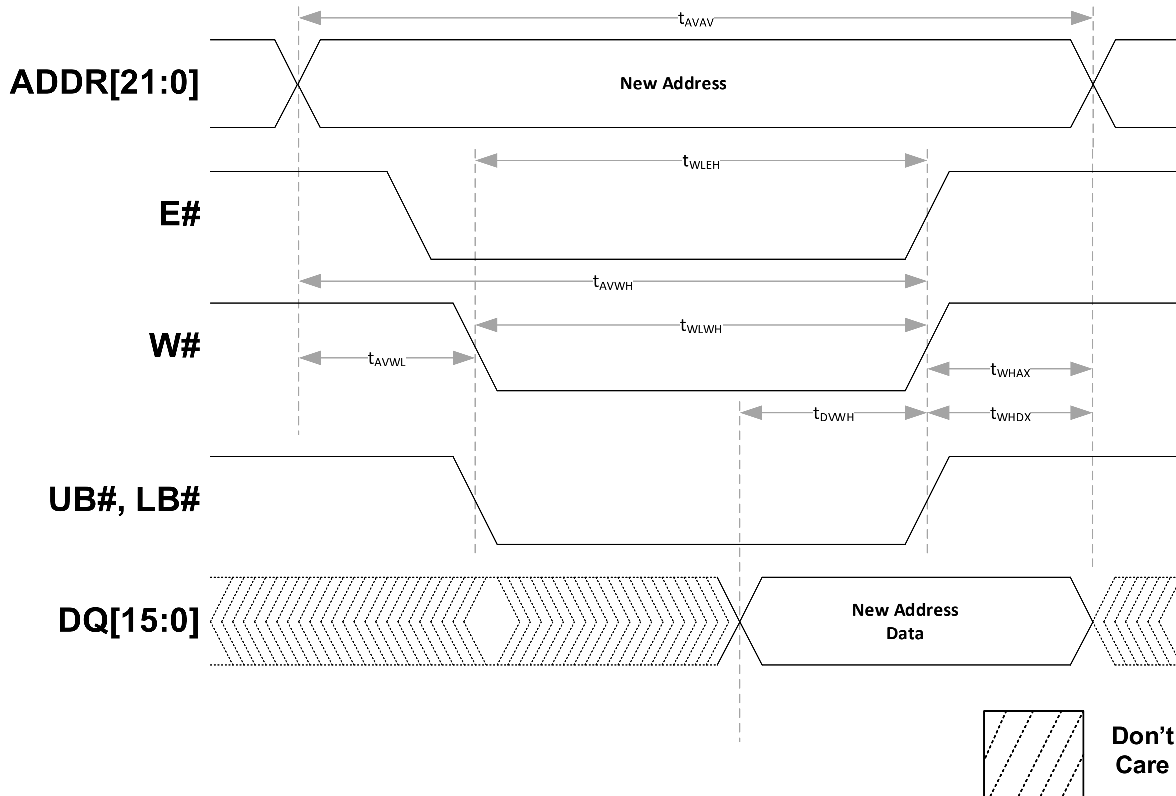


Table 12: Write Operation (W# Controlled)

Parameter	Symbol	Minimum		Maximum	Units
		35ns	45ns		
Write Cycle Time	t_{AVAV}	35	45	-	ns
Address Set-Up Time	t_{AVWL}	0		-	ns
Address Valid to end of Write (G# High)	t_{AVWH}	18	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVWH}	20	30	-	ns
Write Pulse Width (G# High)	t_{WLWH}, t_{WLEH}	15	25	-	ns
Write Pulse Width (G# Low)	t_{WLWH}, t_{WLEH}	15	25	-	ns
Data Valid to end of Write	t_{DVWH}	10	15	-	ns
Data Hold Time	t_{WHDX}	0		-	ns
Write recovery Time	t_{WHAX}	12		-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low
UB# and LB# functionality is not available in the 64Mb device.

Figure 8: Write Operation (E# Controlled)

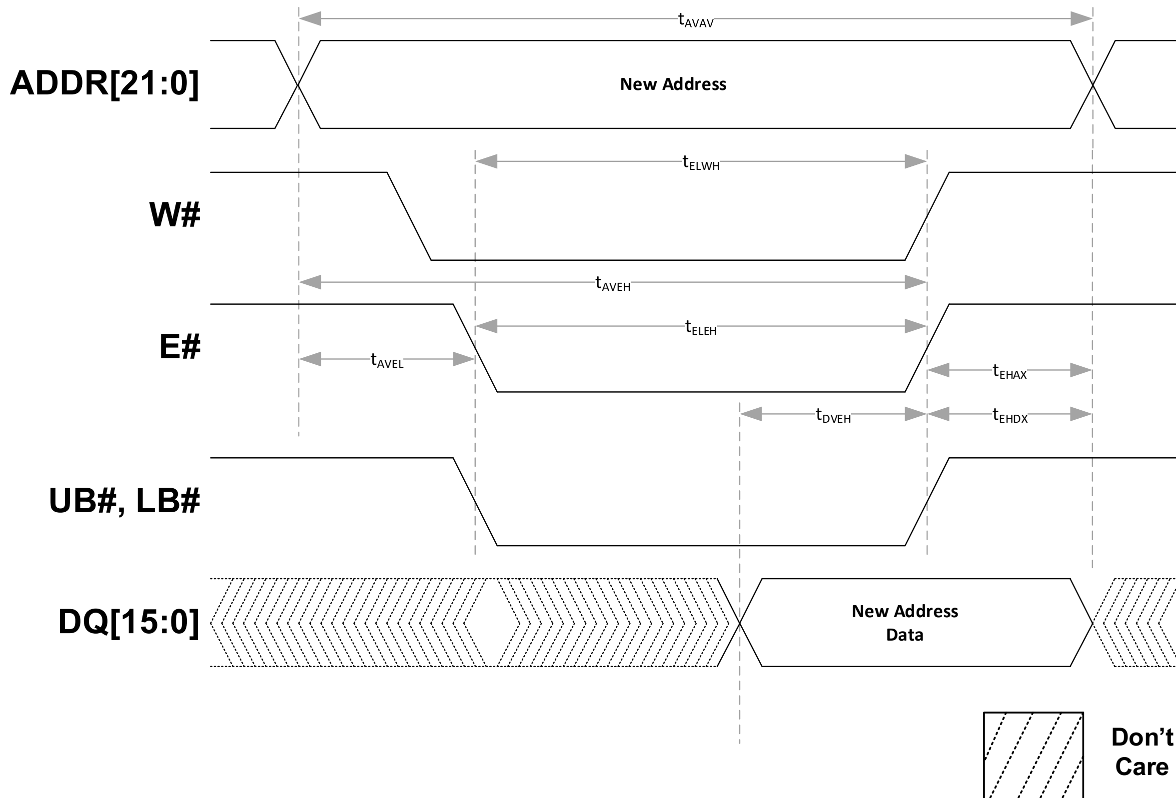


Table 13: Write Operation (E# Controlled)

Parameter	Symbol	Minimum		Maximum	Units
		35ns	45ns		
Write Cycle Time	t_{AVAV}	35	45	-	ns
Address Set-Up Time	t_{AVEL}	0		-	ns
Address Valid to end of Write (G# High)	t_{AVEH}	18	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVEH}	20	30	-	ns
Write Pulse Width (G# High)	t_{ELWH}, t_{ELEH}	15	25	-	ns
Write Pulse Width (G# Low)	t_{ELWH}, t_{ELEH}	15	25	-	ns
Data Valid to end of Write	t_{DVEH}	10	15	-	ns
Data Hold Time	t_{EHDX}	0		-	ns
Write recovery Time	t_{EHAX}	12		-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as W# goes low
UB# and LB# functionality is not available in the 64Mb device.

Bus Turnaround Operation – Read to Write

Figure 9: Bus Turnaround Operation

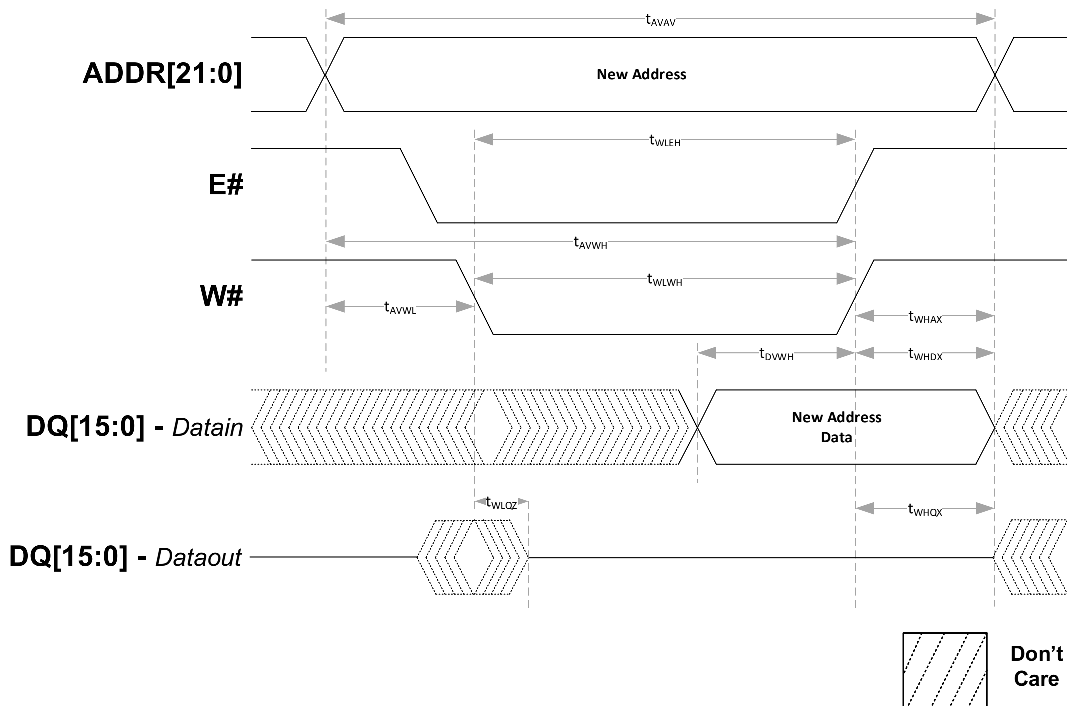


Table 14: Bus Turnaround

Parameter	Symbol	Minimum	Maximum		Units
			35ns	45ns	
W# Low to Data Hi-Z	t_{WLQZ}	0	12	15	ns
W# High to Output Active	t_{WHQX}	3	-		ns

Notes:
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

Read Operation

Figure 10: Read Operation

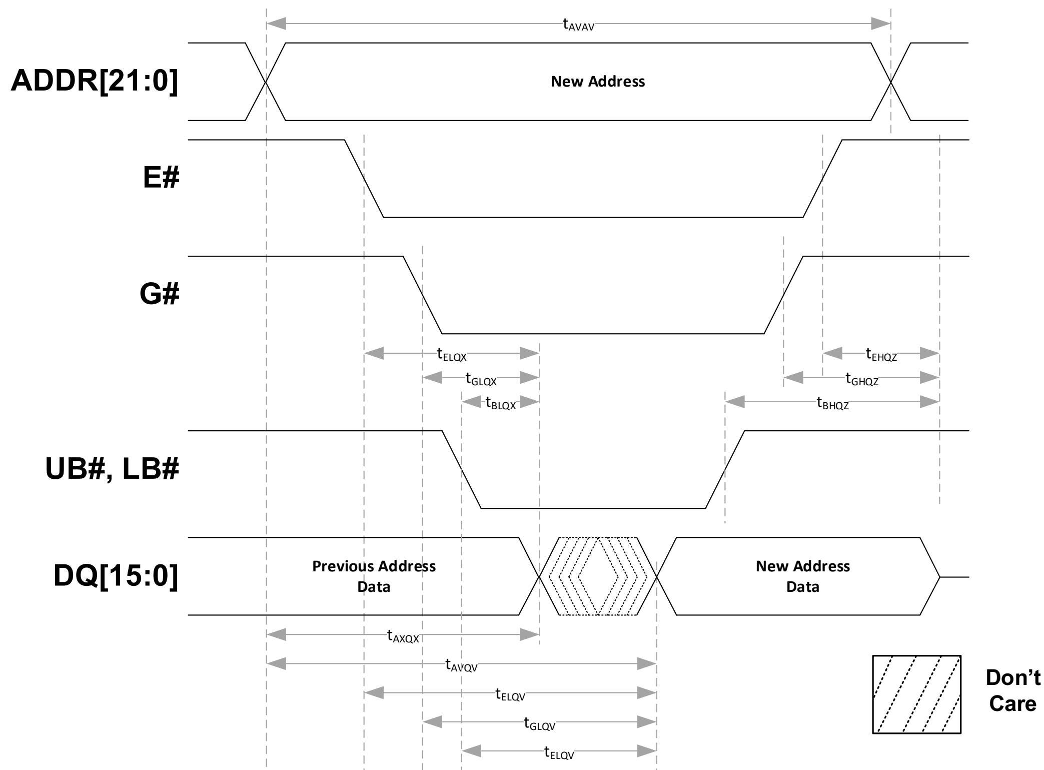


Table 15: Read Operation

Parameter	Symbol	Minimum		Maximum		Units
		35ns	45ns	35ns	45ns	
Read Cycle Time	t_{AVAV}	35	45	-		ns
Address Cycle Time	t_{AVQV}	-		35	45	ns
Chip Enable Access Time	t_{ELQV}	-		35	45	ns
Output Enable Access Time	t_{GLQV}	-		15	25	ns
Byte Enable Access Time	t_{BLQV}	-		15	25	ns
Output Hold From Address Change	t_{AXQX}	3		-		ns
Chip Enable Low to Output Active	t_{ELQX}	3		-		ns
Output Enable Low to Output Active	t_{GLQX}	0		-		ns
Byte Enable Low to Output Active	t_{BLQX}	0		-		ns
Chip Enable High to Output Hi-Z	t_{EHQZ}	0		15		ns
Output Enable High to Output Hi-Z	t_{GHQZ}	0		10	15	ns
Byte Enable High to Output Hi-Z	t_{BHQZ}	0		10		ns

Notes:

W# is High (Logic '1') for Read operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low
UB# and LB# functionality is not available in the 64Mb device.

Endurance and Data Retention

Table 16: Endurance and Data Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{14}	cycles
Data Retention	RET	105°C	10	years
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

Thermal Resistance

Table 17: Thermal Resistance Specifications

Parameter	Description	Test Conditions	44-pin TSOP	54-pin TSOP (1Mb - 16Mb)	54-pin TSOP (32Mb)	48 Ball FBGA (1Mb - 16Mb)	48 Ball FBGA (32Mb)	48 Ball FBGA (64Mb)	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	40.05	52.78	54.07	42.67	43.98	TBD	°C/W
θ_{JC}	Thermal resistance (junction to case)		7.02	6.70	7.82	11.09	11.82	TBD	

Notes:
1: These parameters are guaranteed by characterization; not tested in production.

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Revision History

Revision	Date	Change Summary
REV Q	12/01/2020	Updated Package Drawings – 44-Pin TSOP, 54-Pin TSOP and 48-Ball FBGA Removed “Preliminary” from the footer. Added REACH Compliance
REV R	07/16/2021	Updated max values for I_{READ}, I_{SB}, I_{SLP} in Table 9 (DC Characteristics). Removed Sleep mode SE# functionality. This function has been removed to be 100% functionally compatible with legacy devices. The previously assigned Pin or Ball is now designated as “NC”. Updated Product Use Limitations.
REV S	8/24/2021	Added 64Mb density. Updated max values for I_{READ}, I_{SB}, I_{SLP} in Table 9 (DC Characteristics)